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(54) [Title of the Invention]

DEFECT-PIXEL SENSING DEVICE AND RECORDING MEDIUM WITH RECORDED DEFECT-PIXEL SENSING PROGRAM

(57) [Abstract]

[Problem to be Solved]

When only image data of a pixel included on a specific horizontal line is outputted, means for designating the specific horizontal line is not provided, so that a position of a defect pixel can not be detected, and an high general-purpose defect pixel detecting apparatus can not be provided which deal with an imaging element of a plurality of reading method.

[Solution]

A defect pixel is detected by obtaining a pixel position of the defect pixel depending on a referring step corresponding to a reading mode adopted by image reading means, and comparing the pixel position of the defect pixel with a read pixel position measured by measuring means.

[Claims for the Patent]

[Claim 1]

A defect pixel detecting apparatus, comprising:

image reading means for reading an image signal of a pixel included in an imaging element;

measuring means for measuring a read pixel position by said image reading means;

memorizing means for memorizing a pixel position of a defect pixel in said imaging element, and memorizing a referring step of the pixel position for each reading mode of a pixel; and

defect pixel detecting means for obtaining a pixel position of a defect pixel depending on the referring step corresponding to the reading mode adopted by said image reading means, and comparing the pixel position of the defect pixel with the read pixel position measured by said measuring means to detect the defect pixel.

[Claim 2]

The defect pixel detecting apparatus according to claim 1, characterized by comprising:

correcting means for correcting an image signal of the defect pixel detected by said defect pixel detecting means.

[Claim 3]

The defect pixel detecting apparatus according to claim 1 or claim 2, characterized in that

said memorizing means memorizes a pair of the pixel position of the defect pixel and the referring step.

[Claim 4]

The defect pixel detecting apparatus according to claim 1 or claim 2, characterized in that

the referring step of a pixel position, the referring step being memorized in said memorizing means, is coordinate information indicating an absolute address at which the pixel position of the defect pixel is memorized.

[Claim 5]

The defect pixel detecting apparatus according to claim 1 or claim 2, characterized in that

the referring step of a pixel position, the referring step being memorized in said memorizing means, is coordinate information indicating an relative address at which the pixel position of the defect pixel is memorized.

[Claim 6]

The defect pixel detecting apparatus according to claim 1 or claim 2, characterized in that

the referring step of a pixel position, the referring step being memorized in said memorizing means, is an identifying information indicating whether or not the pixel position is a pixel position of a desired defect pixel.

[Claim 7]

The defect pixel detecting apparatus according to any one of claim 1 to claim 6, characterized by comprising:

temporary storing means for previously reading and temporarily storing the pixel position and the referring step of a defect pixel, the pixel position and the referring step being memorized in said memorizing means, and when the read pixel position is outputted from said measuring means,

outputting the pixel position and the referring step of the defect pixel to said defect pixel detecting means.

[Claim 8]

The defect pixel detecting apparatus according to claim 7, characterized in that

said temporary storing means temporarily stores the pixel positions and the referring steps of a plurality of defect pixels.

[Claim 9]

A recording medium in which a defect pixel detecting program is recorded,

wherein the defect pixel detecting program comprises:

an image reading procedure for reading an image signal of a pixel included in an imaging element;

a measuring procedure for measuring a read pixel position by said image reading procedure;

a memorizing procedure for memorizing a pixel position of a defect pixel in said imaging element, and memorizing a referring step of the pixel position for each reading mode of a pixel; and

a defect pixel detecting procedure for obtaining a pixel position of a defect pixel depending on the referring step corresponding to the reading mode adopted by said image reading procedure, and comparing the pixel position of the defect pixel with the read pixel position measured by said measuring procedure to detect the defect pixel.

[Claim 10]

The recording medium in which the defect pixel detecting program is recorded according to claim 9, characterized by comprising:

a correcting procedure for correcting an image signal of the defect pixel detected by said defect pixel detecting procedure.

[Claim 11]

The recording medium in which the defect pixel detecting program is recorded according to claim 9 or claim 10, characterized in that

said memorizing procedure memorizes a pair of the pixel position of the defect pixel and the referring step.

[Claim 12]

The recording medium in which the defect pixel detecting program is recorded according to claim 9 or claim 10, characterized in that

the referring step of a pixel position, the referring step being memorized in said memorizing procedure, is coordinate information indicating an absolute address at which the pixel position of the defect pixel is memorized.

[Claim 13]

The recording medium in which the defect pixel detecting program is recorded according to claim 9 or claim 10, characterized in that

the referring step of a pixel position, the referring step being memorized in said memorizing procedure, is coordinate information indicating an relative address at which the pixel position of the defect pixel is memorized.

[Claim 14]

The recording medium in which the defect pixel detecting program is recorded according to claim 9 or claim 10, characterized in that

the referring step of a pixel position, the referring step being memorized in said memorizing procedure, is an identifying information indicating whether or not the pixel position is a pixel position of a desired defect pixel.

[Claim 15]

The recording medium in which the defect pixel detecting program is recorded according to any one of claim 9 to claim 14, characterized by comprising:

a temporary storing procedure for previously reading and temporarily storing a pixel position and the referring step of a defect pixel, the pixel position and the referring step being memorized in said memorizing procedure, and when the read pixel position is outputted from said measuring procedure, outputting the pixel position and the referring step of the defect pixel to said defect pixel detecting procedure.

[Claim 16]

The recording medium in which the defect pixel detecting program is recorded according to claim 15, characterized in that

said temporary storing procedure temporarily stores the pixel positions and the referring steps of a plurality of defect pixels.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a defect pixel detecting apparatus detecting a defect pixel in an imaging element and a recording medium in which a defect pixel detecting program is recorded.

[0002]

[Conventional Art]

An element converting light to an electrical signal such as an imaging element includes about hundreds of thousands to millions of pixels on the element. A defect pixel such as a white dead area and a black dead area is included in the pixels. While it is preferable that such a defect pixel is not included, because of a cost problem of a yield ratio and technical difficulty, the element is manufactured as allowing a certain number of defect pixels. As a countermeasure for this problem, such a method, and the like are considered that data of a defect pixel is replaced with data of a previous data of the defect pixel. Thus, it is necessary to identify a defect pixel by comparing position information of the defect pixel with a read position of an imaging element.

[0003]

For example, Figure 24 is a configuration diagram illustrating a conventional defect pixel detecting apparatus disclosed in Japanese Patent Laid-Open No. 63-86971, and in Figure 24, Reference numeral 1 denotes a microcomputer incorporating a EEPROM memorizing a

horizontal line address, a block address, and a cell address at which a defect pixel is included, Reference numeral 2 denotes a bus interface, Reference numerals 3 to 8 denote shift registers, Reference numeral 9 denotes a counter, Reference numeral 10 denotes a timing clock generator generating a timing clock, Reference numeral 11 denotes an imaging element driver controlling a scanning position of a CCD sensor 12 as synchronizing the timing clock, Reference numeral 12 denotes a CCD sensor, an imaging element, Reference numeral 13 denotes a sample hold circuit, Reference numeral 14 denotes an output signal processing circuit outputting image data of pixels included in the CCD sensor 12, Reference numerals 15 to 17 denote counters counting a scanning position of the CCD sensor 12, Reference numerals 18 to 20 denote comparators comparing addresses, and Reference numeral 21 denotes a logical circuit stopping an output of a sample-hold pulse when receiving address match signals from the comparators 18 to 20.

[0004]

Next, an operation will be described. A horizontal line address, a block address, and a cell address (hereinafter, referred to as a defect address) including a defect pixel are previously memorized in the microcomputer 1, after an electric power source is turned on, the defect address is loaded to the shift registers 3 to 8 through the bus interface 2.

[0005]

At this time, as the counter 9 manages the number of the transferred defective addresses, an address of the defect pixel which is first scanned of the defect pixels included in the CCD sensor 12 is loaded to the shift registers 6 to 8, and an address of the defect pixel which is next scanned is loaded to the shift registers 3 to 5.

[0006]

After that, the counters 15 to 17 manage a scanning position of the CCD sensor 12, and if the scanning position of the CCD sensor 12 matches with the defect address loaded in the shift registers 6 to 8, all of the comparators 18 to 20 output address matching signals. Thereby, if receiving the address matching signals from all of the comparators 18 to 20, the logical circuit 21 stops an output of the sample-hold pulse, so that the sample hold circuit 13 does not output image data of a defect pixel, which is outputted from the CCD sensor 12, to the output signal processing circuit 14, but sequentially outputs image data which is just before the defect pixel to the output signal processing circuit 14.

[0007]

Thereby, the output signal processing circuit 14 outputs the image data which is just before the defect pixel as image data of the defect pixel. Meanwhile, if all of the comparators 18 to 20 output the address matching signals, the next defective address loaded in the shift registers 3 to 5 is shifted to the shift registers 6 to 8, and the same processing as the above is repeated again.

[0008]

[Problems to be Solved by the Invention]

The problem is as follows. Since the conventional defect pixel detecting apparatus is configured as described above, when image data of all pixels included in the CCD sensor 12 is outputted, a position of a defect pixel is sequentially detected, and image data can be corrected, however, when only image data of a pixel existing on a specific horizontal line is outputted, means for designating the specific horizontal line is not provided, so that a position of the defect pixel can not be detected, and a high general-purpose defect pixel detecting apparatus corresponding to imaging elements of a variety of reading methods can not be provided.

[0009]

The present invention is invented to solve the above problem, and an object of the present invention is to obtain a high general-purpose defect pixel detecting apparatus which can correspond to imaging elements of a variety of reading methods.

[0010]

[Means for Solving the Problems]

A defect pixel detecting apparatus according to the present invention obtains a pixel position of a defect pixel depending on a referring step corresponding to a reading mode adopted by an image reading mean, and detects the defect pixel by comparing a pixel position of the defect pixel with a read pixel position measured by measuring means.

[0011]

The defect pixel detecting apparatus according to the present invention is provided with correcting means for correcting an image signal of a defect pixel detected by defect pixel detecting means.

[0012]

The defect pixel detecting apparatus according to the present invention memorizes a pair of a pixel position of a defect pixel and the referring step.

[0013]

The defect pixel detecting apparatus according to the present invention causes the referring step of a pixel position memorized in memorizing means to be coordinate information indicating an absolute address at which a pixel position of a defect pixel is memorized.

[0014]

The defect pixel detecting apparatus according to the present invention causes the referring step of a pixel position memorized in memorizing means to be coordinate information indicating a relative address at which a pixel position of a defect pixel is memorized.

[0015]

The defect pixel detecting apparatus according to the present invention causes the referring step of a pixel position memorized in memorizing means to be identifying information indicating whether or not the pixel position is a pixel position of a desired defect pixel.

[0016]

The defect pixel detecting apparatus according to the present invention is provided with temporary storing means for previously reading and temporarily storing a pixel position and the referring step of a defect pixel memorized in the memorizing means, and when the read pixel position is outputted from the measuring means, outputting the pixel position and the referring step of the defect pixel to the defect pixel detecting means.

[0017]

In the defect pixel detecting apparatus according to the present invention, the temporary storing means temporarily stores pixel positions and the referring steps of a plurality of defect pixels.

[0018]

A recording medium in which a defect pixel detecting program according to the present invention is recorded records a defect pixel detecting procedure which obtains a pixel position of a defect pixel depending on a referring step corresponding to a reading mode adopted by an image reading procedure, and detects the defect pixel by comparing a pixel position of the defect pixel with a read pixel position measured by the measuring means.

[0019]

The recording medium in which a defect pixel detecting program according to the present invention is recorded is provided with a correcting procedure for correcting an image signal of a defect pixel detected by the defect pixel detecting procedure.

[0020]

The recording medium in which a defect pixel detecting program according to the present invention is recorded memorizes a pair of a pixel position and the referring step of a defect pixel.

[0021]

In the recording medium in which a defect pixel detecting program according to the present invention is recorded, the referring step of a pixel position memorized in a memorizing procedure is coordinate information indicating an absolute address at which a pixel position of a defect pixel is memorized.

[0022]

In the recording medium in which a defect pixel detecting program according to the present invention is recorded, the referring step of a pixel position memorized in the memorizing procedure is coordinate information indicating a relative address at which a pixel position of a defect pixel is memorized.

[0023]

In the recording medium in which a defect pixel detecting program according to the present invention is recorded, the referring step of a pixel position memorized in the memorizing procedure is identifying information indicating whether or not the pixel position is a pixel position of a desired defect pixel.

[0024]

The recording medium in which a defect pixel detecting program according to the present invention is recorded is provided with temporary storing procedure for previously reading and temporarily storing a pixel position and the referring step of a defect pixel memorized in the memorizing procedure, and when the read pixel position is outputted from a measuring procedure, outputting the pixel position and the referring step of the defect pixel to a defect pixel detecting procedure.

[0025]

In the recording medium in which a defect pixel detecting program according to the present invention is recorded, the temporary storing procedure temporarily stores pixel positions and the referring steps of a plurality of defect pixels.

[0026]

[Embodiments of the Invention]

Hereinafter, an embodiment of the present invention will be described.

[Embodiment 1]

Figure 1 a configuration diagram illustrating a defect pixel detecting apparatus according to an embodiment 1 of the present invention, and in Figure 1, Reference numeral 31 denotes a lens system focusing an optical image of an object, Reference numeral 32 denotes an imaging element being provided with all pixel reading mode and a high rate reading mode, and photo-electrically converting the object image focused by the lens system 31 to output an electrical signal,

Reference numeral 33 denotes an analog processing unit executing an analog processing such as amplifying and digital clamping for the electrical signal outputted from the imaging element 32, and Reference numeral 34 denotes an A/D converter converting an analog signal outputted from the analog processing unit 33 to a digital signal. Meanwhile, image reading means is configured with the analog processing unit 33 and the A/D converter 34.

[0027]

Reference numeral 35 denotes a timing generator driving the imaging element 32 at a timing depending on a reading mode of the imaging element 32, and Reference numeral 36 denotes a pixel position measuring unit measuring a position address of an imaging surface depending on the reading mode of the imaging element 32. Meanwhile, measuring means is configured with the timing generator 35 and the pixel position measuring unit 36.

[0028]

Reference numeral 40a denotes a defect pixel position memory which registers position information of a defect pixel of 24-bit in total of vertical and horizontal, and can register a maximum of 256 defect pixel positions. Reference numeral 40b denotes an address memory which is used in a high rate reading mode, and designates an eight-bit absolute address of the defect pixel position memory 40a registering position information of a defect pixel, Reference numeral 41 denotes a memory controlling circuit controlling the defect pixel position memory 40a and the address memory 40b,

and Reference numeral 42 denotes a defect pixel position register (temporary storing means) temporarily memorizing position information of a defect pixel read from the defect pixel position memory 40a through the memory controlling circuit 41. Meanwhile, memorizing means is configured with the defect pixel position memory 40a, the address memory 40b, and the memory controlling circuit 41.

[0029]

Reference numeral 43 denotes a defect pixel detecting unit (defect pixel detecting means) comparing a position address of an imaging surface of the imaging element 32, the position address being outputted from the pixel position measuring unit 36, and position information of a defect pixel, the position information being stored in the defect pixel position register 42, and when both corresponds to each other, outputting a defect pixel detection signal indicating that a pixel of the position address is a defect pixel. Reference numeral 44 denotes the defect pixel detection signal outputted from the defect pixel detecting unit 43. Reference numeral 45 denotes a defect pixel correcting unit (correcting means) correcting a defect pixel by executing a simple linear interpolation from two same color factor adjacent pixels based on the defect pixel detection signal 44 for 12-bit digital image data outputted from the A/D converter 34.

[0030]

Meanwhile, in Figure 1, while such an case is described that the image reading means, the measuring means, the

memorizing means, the defect pixel detecting means, and the correcting means are configured by hardware, such means may be configured by software, that is, a defect pixel detecting program may be recorded in a computer-readable recording medium, the defect pixel detecting program being configured with an image reading procedure, a measuring procedure, a memorizing procedure, a defect pixel detecting procedure, and a correcting procedure.

[0031]

Next, operations will be described. First, the imaging element 32 correcting a defect pixel will be described. In recent years, the high density of pixels of the imaging element 32 has been advanced. Thus, a time tends to increase to read image data from the imaging element 32. For example, this reduces the responsibility in case of an adjustment of an image angle, so-called, a finder operation in a digital still camera. Thus, recently, the imaging element 32 has been productized, which is provided with two modes such as an all pixel reading mode which reads all pixel data as giving priority to image quality in case of the normal photographing, and a high rate reading mode which thins in a vertical direction as giving priority to a reading rate in case of a finder operation. While a variety of reading methods are included in such two modes, here, two kinds of reading methods for each mode will be described as examples.

[0032]

Figure 2 illustrates a part of an imaging element surface of the progressive scan method in the all pixel reading mode,

and Figure 3 illustrates a part of an imaging surface of the field reading method in the all pixel reading mode, Figure 4 illustrates a part of an imaging surface of a vertical simple thinning method in the high rate reading mode, and Figure 5 illustrates a part of an imaging surface of a vertical two pixel adding method in the high rate reading mode. In such figures, a black circle illustrates a position of a defect pixel, and a number attached to the black circle indicates a registering order of defect pixel position information which will be described later. Meanwhile, it is assumed that the imaging element 32 is a two-dimensional CCD sensor of 4096-pixel × 4096-row, and outputted digital image data is 12-bit.

[0033]

The progressive scan method of Figure 2 is such a method that image data of each pixel is read from left to right in the figure in a horizontal direction, and from the first line in order of upper to down in a vertical direction.

[0034]

The field reading method of Figure 3 is a four field reading method, and reads in order of left to right in the figure in a horizontal direction as the progressive scan method. In a vertical direction, first, image data of each pixel is read for each field in order of the first field, the second field, up to the fourth field. In Figure 2, after the first fields of 1 line, 5 line, and 9 line are read, the second fields of 2 line, 6 line, and 10 line are read,

and finally, the fourths of as 4 line, 8 line, and 12 line are read.

[0035]

The vertical simple thinning method of Figure 4 reads in order of left to right in the figure in a horizontal direction as the all pixel reading mode. In a vertical direction, by designating eight lines as one unit, the second line and the seventh line, diagonal line areas, are read. In Figure 4, image data of each pixel is read in order of the second line, the seventh line, the tenth line, the fifteenth line, eighteenth line, and like.

[0036]

The vertical two pixel adding method of Figure 5 reads in order of left to right in the figure in a horizontal direction as the all pixel reading mode. In a vertical direction, by designating 12 lines as one unit, two vertical pixels of the first line and the third line, diagonal areas, are added, and two vertical pixels of the eighth line and the tenth line, diagonal areas, are added, and the averages are read out. In Figure 5, the averages of two vertical pixels of the first line and the third line, the eighth line and the tenth line, the thirteenth line and the fifteenth line, and the twentieth line and the twenty second line are read out.

[0037]

Figure 6 illustrates the defect pixel position memory 40a. It is assumed that the registered defect pixel position information indicates an absolute position of a screen.

Thus, when a two-dimensional CCD sensor of 4096-pixel × 4096-row is used, one piece of defect pixel position information is configured with 24-bit width in total of 12-bit (0 to 4095) in a horizontal direction, and 12-bit (0 to 4095) in a vertical direction. The defect pixel position memory 40a includes an address space of eight-bit, so that a maximum of 256 pieces of defect pixel position information can be registered.

[0038]

It is assumed that an order for registering the defect pixel position information is a reading order in the all pixel reading mode. That is, when an imaging element of the progressive scan method of Figure 2 is used, the defect pixel position information is registered from address 0 in order of left upper to right down in the figure such as D1, D2, D3, D4, and the like, when an imaging element of the field reading method of Figure 3 is used, in consideration of only an area illustrated in Figure 3, the defect pixel position information is registered in order of D1, D2, D3, D4 (the first field), D5, D6, D7, D8, D9 (the second field).

[0039]

Figure 7 illustrates the address memory 40b of the vertical simple thinning method, Figure 8 illustrates the address memory 40b of the vertical two pixel adding method, and the defect pixel position information used in the high rate reading mode is read from the defect pixel position memory 40a. It is assumed that an order for registering a defect pixel position memory address to the address memory

40b is a reading order in the high rate reading mode. That is, when an imaging element of the vertical simple thinning method of Figure 4 is used, the defect pixel position memory address is registered from address 0 in order of the defect pixel position memory addresses 2, 3, 9, 13, and the like at which D3, D4, D10, D14, and the like are registered, and when an imaging element of the vertical two pixel adding method of Figure 5 is used, as illustrated in Figure 8, the defect pixel position memory address is registered in order of the defect pixel position memory address 4, 5, 0, 1, and the like at which D5, D6, D1, D2, D7, and the like are registered.

[0040]

Next, a detailed configuration and a detailed operation of the all pixel reading mode will be described. When the all pixel reading mode is started by a not-illustrated switch, a not-illustrated shutter, or the like, the timing generator 35 generates a timing clock for driving the imaging element 32.

[0041]

The imaging element 32 outputs an imaging signal depending on the strength of light, and the imaging signal passes through the analog processing unit 33 to be converted to a digital image signal by the A/D converter 34, and is transferred to the defect pixel correcting unit 45. At the same time, when the timing generator 35 generates a pixel clock synchronized to the timing clock, the pixel position measuring unit 36 measures the pixel clock. The pixel

position measuring unit 36 is provided with a counter of 24-bit in total of 12-bit (o to 4095) in a horizontal direction, and 12-bit (o to 4095) in a vertical direction so as to be able to count all pixels, and the counted result indicates an absolute position in one screen by incrementing the counter by one pixel clock in the all pixel reading mode. The measured result is sequentially transferred to the defect pixel detecting unit 43.

[0042]

ON the other hand, position information of D1 of address 0, which is the first defect pixel of the all pixel reading mode, is transferred from the defect pixel position memory 40a to the defect pixel detecting unit 43 through the defect pixel position register 42. The defect pixel detecting unit 43 compares the position information with the measured result sequentially transferred from the pixel position measuring unit 36, and when both correspond to each other, outputs the defect pixel detection signal 44. Based on this signal, the defect pixel correcting unit 45 replaces an image signal of the defect pixel D1 of digital image signals with a value which is linearly interpolated by using an image signal of the two same color factor adjacent pixels in a horizontal direction.

[0043]

At the same time, the defect pixel detection signal 44 outputted from the defect pixel detecting unit 43 is transferred to the memory controlling circuit 41, and position information of D2 of address 1, which becomes next

defect pixel, is read from the defect pixel position memory 40a. The read position information of D2 is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42. The defect pixel detecting unit 43 compares the measured result sequentially transferred from the pixel position measuring unit 36 with the position information of D2, and when both correspond to each other, outputs the defect pixel detection signal 44 again.

[0044]

As described above, hereinafter, the defect pixels D3, D4, D5, and the like, and the defect pixels in the all pixel reading mode are detected and corrected by starting reading from address 0 of the defect pixel position memory 40a, and repeating an operation for incrementing by one an address of the defect pixel position memory 40a every time the defect pixel detection signal 44 is outputted.

[0045]

Next, a detailed configuration and a detailed operation of the high rate reading mode will be described. First, the configuration and operation of the vertical simple thinning method of Figure 4 will be described. When the high rate reading mode is started by a not-illustrated switch, a not-illustrated shutter, or the like, the timing generator 35 generates a timing clock for driving the imaging element 32.

[0046]

The imaging element 32 outputs an imaging signal depending on the strength of light, and the imaging signal

passes through the analog processing unit 33 to be converted to a digital image signal by the A/D converter 34, and is transferred to the defect pixel correcting unit 45. At the same time, when the timing generator 35 generates a pixel clock synchronized to the timing clock, the pixel position measuring unit 36 measures the pixel clock. At this time, in the vertical simple thinning method of Figure 4, by designating eight lines as a unit in a vertical direction, only the second line and the seventh line are read, so that the counter in a vertical direction is measured as indicating absolute positions of one screen as 2, 7, 10, 15, 18, and the like. The measured result is sequentially transferred to the defect pixel detecting unit 43.

[0047]

On the other hand, when the high rate reading mode is started, as illustrated in Figure 7, eight-bit address information "address 2" registered in address 0 of the address memory 40b, i.e., an address of the defect pixel position memory 40a, at which D3, which is first used in the vertical simple thinning method, is registered, is transferred by the memory controlling circuit 41 to the defect pixel position memory 40a. The read position information of D3 of "address 2" in the defect pixel position memory 40a is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42. The defect pixel detecting unit 43 compares the position information with the measured result sequentially transferred from the pixel position measuring unit 36, and when both corresponds

to each other, outputs the defect pixel detection signal 44. Based on this signal, the defect pixel correcting unit 45 replaces an image signal of the defect pixel D3 of digital image signals with a value which is linearly interpolated by using an image signal of the two same color factor adjacent pixels in a horizontal direction.

[0048]

At the same time, the defect pixel detection signal 44 outputted from the defect pixel detecting unit 43 is transferred to the memory controlling circuit 41, and the eight-bit address information "address 3" registered in address 1 of the address memory 40b, i.e., an address of the defect pixel position memory 40a, at which D4, which is next used in the vertical simple thinning method, is registered, is transferred by the memory controlling circuit 41 to the defect pixel position memory 40a. The read position information of D4 of "address 3" in the defect pixel position memory 40a is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42. The defect pixel detecting unit 43 compares the position information with the measured result sequentially transferred from the pixel position measuring unit 36, and when both corresponds to each other, outputs the defect pixel detection signal 44 again.

[0049]

As described above, first, the address information of address 0 of the address memory 40b is transferred to the defect pixel position memory 40a, and such an operation is

repeated that an address of the address memory 40b is incremented by one every time the defect pixel detection signal 44 is outputted. Thereby, hereinafter, the defect pixels D10, D14, and the like, and the defect pixels of the vertical simple thinning method are detected and corrected.

[0050]

Next, the configuration and operation of the vertical two pixel adding method of Figure 5 will be described. When the high rate reading mode is started by a not-illustrated switch, a not-illustrated shutter, or the like, the timing generator 35 generates a timing clock for driving the imaging element 32.

[0051]

The imaging element 32 outputs an imaging signal depending on the strength of light, and the imaging signal passes through the analog processing unit 33 to be converted to a digital image signal by the A/D converter 34, and is transferred to the defect pixel correcting unit 45. At the same time, when the timing generator 35 generates a pixel clock synchronized to the timing clock, the pixel position measuring unit 36 measures the pixel clock. At this time, in the vertical two pixel adding method of Figure 5, by designating 12 lines as a unit, two vertical pixels of the first line and the third line, and the eighth line and the tenth line are added, and the averages are read out. Thus, the counter in a vertical direction measures by using any line of the two lines to be added such as 1, 8, 13, 20, and

the like as a criterion. The measured result is sequentially transferred to the defect pixel detecting unit 43.

[0052]

On the other hand, when the high rate reading mode is started, as illustrated in Figure 8, the eight-bit address information "address 4" registered in address 0 of the address memory 40b, i.e., an address of the defect pixel position memory 40a, at which D5, which is first used in the vertical two pixel adding method, is registered, is transferred by the memory controlling circuit 41 to the defect pixel position memory 40a. The read position information of D5 of "address 4" in the defect pixel position memory 40a is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42.

[0053]

Here, while only the measured results of 1, 8, 13, 20, and the like are outputted as the criterion lines from the pixel position measuring unit 36, to detect defect pixels included in two lines at the same time, a comparison condition is newly generated in the defect pixel detecting unit 43, which is obtained by adding two to the criterion line, i.e., 3, 10, 15, 22, and the like. Thereby, when position information from the defect pixel position memory 40a corresponds to the criterion line or the criterion line + 2, the defect pixel detecting unit 43 becomes able to output the defect pixel detection signal 44. In case of D5, D5 is included in the third line in an absolute position of one screen, so that "1", a criterion line, is outputted from

the pixel position measuring unit 36, and corresponds to the third line under the comparison condition of the criterion line + 2, and the defect pixel detection signal 44 is outputted. When the defect pixel detection signal 44 is outputted, the defect pixel correcting unit 45 replaces an image signal of the defect pixel D5 of digital image signals with a value which is linearly interpolated by using an image signal of the two same color factor adjacent pixels in a horizontal direction.

[0054]

At the same time, the defect pixel detection signal 44 outputted from the defect pixel detecting unit 43 is transferred to the memory controlling circuit 41, and the eight-bit address information "address 5" registered in address 1 of the address memory 40b, i.e., an address of the defect pixel position memory 40a, at which D6, which is next used in the vertical two pixel adding method, is registered is transferred by the memory controlling circuit 41 to the defect pixel position memory 40a. The read position information of D6 of address 5 of the defect pixel position memory 40a is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42. The defect pixel detecting unit 43 generates a comparison condition based on the measured result sequentially transferred from the pixel position measuring unit 36, and when both correspond to each other, outputs the defect pixel detection signal 44 again.

[0055]

As described above, to detect defect pixels included in two lines in the defect pixel detecting unit 43, a comparison condition is added based on the measured result from the pixel position measuring unit 36. The address information of address 0 of the address memory 40b is transferred to the defect pixel position memory 40a, and such an operation is repeated that an address of the address memory 40b is incremented by one every time the defect pixel detection signal 44 is outputted. Thereby, hereinafter, the defect pixels D1, D2, D7, and the like, and the defect pixels in the vertical two pixel adding method are detected and corrected.

[0056]

As apparent from the above, according to the embodiment 1, by including the address memory 40b for detecting a defect pixel in the high rate mode, it becomes unnecessary to register position information of a defect pixel for the all pixel reading mode and the high rate reading mode respectively, so that a memory capacity can be reduced.

[0057]

Meanwhile, in the embodiment 1, while it is assumed that the imaging element includes 4096-pixel × 4096-row, the number of pixels may be arbitrary, and the number of bits of the pixel counter may be changed depending on the number of pixels. The number of detected defect pixels to be registered may be also arbitrary, and a memory capacity may be changed.

[0058]

While the defect pixel position register 42 of the embodiment 1 memorizes a pixel of defect pixel position information, by including a plurality of pixels of capacity, based on information of the address memory 40b before detecting a defect pixel, a plurality of pixels of defect pixel position information becomes able to be previously read, and even when the reading rate of the defect pixel position memory 40a is slow, a defect pixel becomes able to be detected in real time.

[0059]

Furthermore, while the embodiment 1 is applied to an inputting device, an imaging element, the present invention may be applied to detect a defect pixel of a displaying device such as a liquid crystal and a plasma display, and the same advantageous effect as that of the embodiment 1 may be obtained.

[0060]

[Embodiment 2]

Figure 9 is a configuration diagram illustrating a defect pixel detecting apparatus according to an embodiment 2 of the present invention, and in Figure 9, the same code as that of Figure 1 indicates the same unit as that of Figure 1 or the corresponding unit to that of Figure 1, so that the description will be omitted. Reference numeral 40 denotes a memory registering position information of a defect pixel of 24-bit in total of vertical and horizontal directions, and an eight-bit address at which defect pixel position information used in a high rate reading mode is

registered, and an address/defect pixel position memory (memorizing means) which can register a maximum of 256 pieces of defect pixel position information. Reference numeral 50 denotes a start address memory registering an address of the defect pixel position information which is first read in the high rate reading mode, and Reference numeral 51 denotes a memory address register (temporary storing means) in which an address read from the address/defect pixel position memory 40 through the memory controlling circuit 41 is temporarily memorized.

[0061]

Next, an operation will be described. In the embodiment 1, while such a case is described that the address memory 40b registering coordinate information, a detecting procedure, and the defect pixel position memory 40a registering position information of a defect pixel are provided respectively, a pair of the position information and the coordinate information of a defect pixel may be registered in the same memory.

[0062]

Figure 10 illustrates the address/defect pixel position memory 40 when an imaging element of the vertical simple thinning method of Figure 4 is used, and Figure 11 illustrates the address/defect pixel position memory 40 when an imaging element of the vertical two pixel adding method of Figure 5 is used. Eight-bit address space is included, and a maximum of 256 pieces of defect pixel position information can be registered. A data width is designated

as 32-bit, and the defect pixel position information is registered in the lower part [23:0]. An address is registered in the upper part [31:24], at which the defect pixel position information to be next detected in the high rate reading mode is included. That is, this eight-bit address is once read outside the address/defect pixel position memory 40, and indicates an address of the address/defect pixel position memory 40.

[0063]

It is assumed that the defect pixel position information registered in the lower part [23:0] of Figure 10 and Figure 11 indicates an absolute position in one screen in the all pixel reading mode. Thus, a two-dimensional CCD sensor of 4096-pixel × 4096-row is used, a bit width of one piece of defect pixel position information is 24 in total of 12-bit (0 to 4095) in a horizontal direction, and 12-bit (0 to 4095) in a vertical direction.

[0064]

It is assumed that a registering order of the defect pixel position information is a reading order in the all pixel reading mode. That is, when an imaging element of the progressive scan method of Figure 2 is used, the defect pixel position information is registered from address 0 in order of left upper to right down of the figure of D1, D2, D3, D4, and the like, and when an imaging element of the field reading method of Figure 3 is used, in consideration of only the area illustrated in Figure 3, the defect pixel position information is registered in order of D1, D2, D3,

and D4 (the first field), and D5, D6, D7, D8, and D9 (the second field).

[0065]

The upper part [31:24] of Figure 10 illustrates an address registering method of the vertical simple thinning method of Figure 4, and indicates a reading order of the defect pixel position information used in the high rate reading mode. In case of the vertical simple thinning method of Figure 4, defect pixels to be detected are D3, D4, D10, D14, and the like, and only an address of D3 to be first used of the address/defect pixel position memory 40 is designated as address 2 by the start address memory 50. Thus, an address 3 of D4 to be next used is registered in the upper part [31:24] of the address 2, and an address 9 of D10 to be further next used is registered in the upper part [31:24] of the address 3, and similarly, an address at which the defect pixel position information to be next used is registered is registered in the upper part [31:24].

[0066]

The upper part [31:24] of Figure 11 illustrates the address registering method of the vertical two pixel adding method of Figure 5, and indicates a reading order of the defect pixel position information used in the high rate reading mode. In case of the vertical simple thinning method of Figure 5, defect pixels to be detected are D5, D6, D1, D2, and the like, and only an address of D5 to be first used of the address/defect pixel position memory 40 is designated as address 4 by the start address memory 50. Thus, an address

5 of D6 to be next used is registered in the upper part [31:24] of the address 4, and an address 0 of D1 to be further next used is registered in the upper part [31:24] of the address 5, and similarly, an address at which the defect pixel position information to be next used is registered is registered in the upper part [31:24].

[0067]

Next, a detailed configuration and a detailed operation of the all pixel reading mode will be described. When the all pixel reading mode is started by a not-illustrated switch, a not-illustrated shutter, or the like, the timing generator 35 generates a timing clock for driving the imaging element 32.

[0068]

The imaging element 32 outputs an imaging signal depending on the strength of light, and the imaging signal passes through the analog processing unit 33 to be converted to a digital image signal by the A/D converter 34, and is transferred to the defect pixel correcting unit 45. At the same time, when the timing generator 35 generates a pixel clock synchronized to the timing clock, the pixel position measuring unit 36 measures the pixel clock. The pixel position measuring unit 36 includes a counter of 24-bit in total of 12-bit (0 to 4095) in a horizontal direction, and 12-bit (0 to 4095) in a vertical direction, and by incrementing by one with the image clock in the all image reading mode, the counted result indicates an absolute

position in one screen. The measured result is sequentially transferred to the defect pixel detecting unit 43.

[0069]

On the other hand, the position information of D1 of address 0 [23:0] which is the first defect pixel in the all pixel reading mode is transferred from the address/defect pixel position memory 40 to the defect pixel detecting unit 43 through the defect pixel position register 42. The defect pixel detecting unit 43 compares the position information with the measured result sequentially transferred from the pixel position measuring unit 36, and when both corresponds to each other, outputs the defect pixel detection signal 44. Based on this signal, the defect pixel correcting unit 45 replaces an image signal of the defect pixel D1 of digital image signals with a value which is linearly interpolated by using an image signal of the two same color factor adjacent pixels in a horizontal direction.

[0070]

At the same time, the defect pixel detection signal 44 outputted from the defect pixel detecting unit 43 is transferred to the memory controlling circuit 41, and position information of D2 of address 1 [23:0], which becomes next defect pixel, is read from the address/defect pixel position memory 40. The read position information of D2 is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42. The defect pixel detecting unit 43 compares the measured result sequentially transferred from the pixel position measuring unit 36 with

the position information of D2, and when both correspond to each other, outputs the defect pixel detection signal 44 again.

[0071]

As described above, hereinafter, the defect pixels D3, D4, D5, and the like, and the defect pixels in the all pixel reading mode are detected and corrected by starting reading the defect pixel position information of the lower part [23:0] from address 0 of the address/defect pixel position memory 40, and repeating an operation for incrementing by one an address of the address/defect pixel position memory 40 every time the defect pixel detection signal 44 is outputted.

[0072]

Next, a detailed configuration and a detailed operation of the high rate reading mode will be described. First, the configuration and operation of the vertical simple thinning method of Figure 4 will be described. When the high rate reading mode is started by a not-illustrated switch, a not-illustrated shutter, or the like, the timing generator 35 generates a timing clock for driving the imaging element 32.

[0073]

The imaging element 32 outputs an imaging signal depending on the strength of light, and the imaging signal passes through the analog processing unit 33 to be converted to a digital image signal by the A/D converter 34, and is transferred to the defect pixel correcting unit 45. At the

same time, when the timing generator 35 generates a pixel clock synchronized to the timing clock, the pixel position measuring unit 36 measures the pixel clock. At this time, in the vertical simple thinning method of Figure 4, by designating eight lines as a unit in a vertical direction, only the second line and the seventh line are read, so that the counter in a vertical direction is measured as indicating absolute positions of one screen as 2, 7, 10, 15, 18, and the like. The measured result is sequentially transferred to the defect pixel detecting unit 43.

[0074]

On the other hand, when the high rate reading mode is started, the address information "address 2" of the start address memory 50, i.e., an address of the address/defect pixel position memory 40, at which D3, which is first used in the vertical simple thinning method, is registered, is transferred by the memory controlling circuit 41 to the address/defect pixel position memory 40. The read position information [23:0] of D3 of "address 2" in the address/defect pixel position memory 40 is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42. At the same time, the address information [31:24] of "address 2" (address 3) is transferred to the memory address register 51.

[0075]

Next, the defect pixel detecting unit 43 compares the defect pixel position register 42 with the measured result sequentially transferred from the pixel position measuring

unit 36, and when both correspond to each other, outputs the defect pixel detection signal 44. Based on this signal, the defect pixel correcting unit 45 replaces an image signal of the defect pixel D3 of digital image signals with a value which is linearly interpolated by using an image signal of the two same color factor adjacent pixels in a horizontal direction.

[0076]

At the same time, the defect pixel detection signal 44 outputted from the defect pixel detecting unit 43 is transferred to the memory controlling circuit 41, and the address information "address 3" of the memory address register is transferred to an address input of the address/defect pixel position memory 40. Thereby, "address 3" of the address/defect pixel position memory 40, i.e., D4 to be next used in the vertical simple thinning method is read. The read position information [23:0] of D4 of "address 3" in the address/defect pixel position memory 40 is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42. At the same time, the address information [31:24] (address 9) of "address 3" is transferred to the memory address register 51. Next, the defect pixel detecting unit 43 compares the defect pixel position register 42 with the measured result sequentially transferred from the pixel position measuring unit 36, and when both correspond to each other, outputs the defect pixel detection signal 44 again.

[0077]

As described above, based on the address information of the start address memory 50, the defect pixel position information which is first necessary, and the address information which is next necessary are read from the address/defect pixel position memory 40. Next, such an operation is repeated that the address information of the memory address register 51 is transferred to the address/defect pixel position memory 40 every time the defect pixel detection signal 44 is outputted. Thereby, the defect pixel position information and the address information are always updated by the defect pixel detection signal 44, and hereinafter, the defect pixels D10, D14, and the like, and the defect pixels in the vertical simple thinning method are detected and corrected.

[0078]

Next, a configuration and an operation of the vertical two pixel adding method of Figure 5, and a timing chart of Figure 12 will be described. When the high rate reading mode is started by a not-illustrated switch, a not-illustrated shutter, or the like, the timing generator 35 generates a timing clock for driving the imaging element 32.

[0079]

The imaging element 32 outputs an imaging signal depending on the strength of light, and the imaging signal passes through the analog processing unit 33 to be converted to a digital image signal by the A/D converter 34, and is transferred to the defect pixel correcting unit 45. At the

same time, when the timing generator 35 generates a pixel clock synchronized to the timing clock, the pixel position measuring unit 36 measures the pixel clock. At this time, in the vertical two pixel adding method of Figure 5, by designating 12 lines as a unit, two vertical pixels of the first line and the third line, and the eighth line and the tenth line are added, and the averages are read out. Thus, the counter in a vertical direction measures by using any line of the two lines to be added such as 1, 8, 13, 20, and the like as a criterion. The measured result is sequentially transferred to the defect pixel detecting unit 43.

[0080]

On the other hand, when the high rate reading mode is started, the address information "address 4" of the start address memory 50, i.e., an address of the address/defect pixel position memory 40, at which D5, which is first used in the vertical simple thinning method, is registered, is transferred by the memory controlling circuit 41 to the address/defect pixel position memory 40. The read position information [23:0] of D5 of "address 4" in the address/defect pixel position memory 40 is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42. At the same time, the address information [31:24] (address 5) of "address 4" is transferred to the memory address register 51.

[0081]

Here, while only the measured results of 1, 8, 13, 20, and the like are outputted as the criterion lines from the

pixel position measuring unit 36, to detect defect pixels included in two lines at the same time, a comparison condition is newly generated in the defect pixel detecting unit 43, which is obtained by adding two to the criterion line, i.e., 3, 10, 15, 22, and the like. Thereby, when position information from the address/defect pixel position memory 40 corresponds to the criterion line or the criterion line + 2, the defect pixel detecting unit 43 becomes able to output the defect pixel detection signal 44.

[0082]

In case of D5, D5 is included in the third line in an absolute position of one screen, so that "1", a criterion line, is outputted from the pixel position measuring unit 36, and corresponds to the third line under the comparison condition of the criterion line + 2, and the defect pixel detection signal 44 is outputted. When the defect pixel detection signal 44 is outputted, the defect pixel correcting unit 45 replaces an image signal of the defect pixel D5 of digital image signals with a value which is linearly interpolated by using an image signal of the two same color factor adjacent pixels in a horizontal direction.

[0083]

At the same time, the defect pixel detection signal 44 outputted from the defect pixel detecting unit 43 is transferred to the memory controlling circuit 41, and the address information "address 5" of the memory address register is transferred to an address input of the address/defect pixel position memory 40. Thereby, "address

5" of the address/defect pixel position memory 40, i.e., D6 which is next used in the vertical simple thinning method is read. The read position information [23:0] of D6 of "address 5" in the address/defect pixel position memory 40 is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42. At the same time, the address information [31:24] (address 0) of "address 5" is transferred to the memory address register 51. Next, the defect pixel detecting unit 43 generates a comparison condition based on the measured result sequentially transferred from the pixel position measuring unit 36, and when both correspond to each other, outputs the defect pixel detection signal 44 again.

[0084]

As described above, to detect defect pixels included in two lines by the defect pixel detecting unit 43, a comparison condition is added based on the measured result from the pixel position measuring unit 36. Furthermore, based on the address information of the start address memory 50, the defect pixel position information which is first necessary, and the address information which is next necessary are read from the address/defect pixel position memory 40. Next, such an operation is repeated that the address information of the memory address register 51 is transferred to the address/defect pixel position memory 40 every time the defect pixel detection signal 44 is outputted. Thereby, the defect pixel position information and the address information are always updated by the defect pixel

detection signal 44, and hereinafter, the defect pixels D1, D2, D7, and the like, and the defect pixels in the vertical two pixel adding method are detected and corrected.

[0085]

As apparent from the above, according to the embodiment 2, by registering the defect pixel position information, and a detecting procedure for detecting a defect pixel in the high rate reading mode in the same memory, a memory area can be effectively used, and it becomes unnecessary to register position information of a defect pixel for the all pixel reading mode and the high rate reading mode respectively, so that a memory capacity can be reduced.

[0086]

Meanwhile, in the embodiment 2, while it is assumed that the imaging element includes 4096-pixel × 4096-row, the number of pixels may be arbitrary, and the number of bits of the pixel counter may be changed depending on the number of pixels. The number of detected defect pixels to be registered may be also arbitrary, and a memory capacity may be changed.

[0087]

Furthermore, while the embodiment 2 is applied to an inputting device, an imaging element, the present invention may be applied to detect a defect pixel of a displaying device such as a liquid crystal and a plasma display, and the same advantageous effect as that of the embodiment 2 may be obtained.

[0088]

[Embodiment 3]

Figure 13 is a configuration diagram illustrating a defect pixel detecting apparatus according to an embodiment 3 of the present invention, and in Figure 13, the same code as that of Figure 9 indicates the same unit as that of Figure 9 or the corresponding unit to that of Figure 9, so that the description will be omitted. Reference numeral 40 denotes a memory registering position information of a defect pixel of 24-bit in total of vertical and horizontal directions, and an four-bit relative address at which defect pixel position information used in a high rate reading mode is registered, and an address/defect pixel position memory which can register a maximum of 256 pieces of defect pixel position information. Reference numeral 60 denotes an address converting unit which converts the four-bit relative address outputted from the address/defect pixel position memory 40 through the memory address register 51 to an eight-bit absolute address of the address/defect pixel position memory 40. Reference numeral 61 denotes an address error signal outputted from the address converting unit 60 when the eight-bit absolute address can not been generated from the four-bit relative address.

[0089]

Next, an operation will be described. In the above embodiments 1 and 2, while an absolute address of a memory is used as detecting procedure information of the high rate reading mode, a relative address of the memory may be used as a detecting procedure.

[0090]

Figure 14 illustrates the address/defect pixel position memory 40 when an imaging element of the vertical simple thinning method of Figure 4 is used, and Figure 15 illustrates the address/defect pixel position memory 40 when an imaging element of the vertical two pixel adding method of Figure 5 is used. The address/defect pixel position memory 40 includes eight-bit address space, and a maximum of 256 pieces of defect pixel position information can be registered. A data width is designated as 28-bit, and the defect pixel position information is registered in the lower part [23:0]. A relative address is registered in the upper part [27:24], at which the defect pixel position information to be next detected in the high rate reading mode is included. This four-bit address is once read outside the address/defect pixel position memory 40, and is converted to an absolute address of the address/defect pixel position memory 40 by the address converting unit 60.

[0091]

The defect pixel position information recorded in the lower part [23:0] of Figure 14 and Figure 15 is the same as that of the above embodiment 2, so that the description will be omitted. The upper part [27:24], four-bit, of Figure 14 and Figure 15 illustrates a relative address registering method in the vertical simple thinning method of Figure 4, and indicates a reading order of the defect pixel position information, which is used in the high rate reading mode. [26:24], three-bit, illustrates a signed relative address,

and can designate an area of -4 to +3, and this three-bit relative address is transferred to the address converting unit 60. In the address converting unit 60, after a value of an address of the address/defect pixel position memory 40, which is currently being read, is converted to an absolute address by adding a relative address to the value, the absolute address is transferred to the address/defect pixel position memory 40 through the memory controlling circuit 41. When the relative address can not be represented in the area of -4 to +3, [28], one bit, is notified as "High" to the address converting unit 60.

[0092]

In case of the vertical simple thinning method of Figure 4, defect pixels to be detected are D3, D4, D10, D14, and the like, and an address of D3 to be first used of the address/defect pixel position memory 40 is designated as address 2 by the start address memory 50. Thus, a relative address (3 (address) - 2 (address) = +1) of D4 of address 3 to be next used is registered in the upper part [26:24] of address 2. While a relative address of D10 of address 9 to be next used is registered in the upper part [26:24] of address 3, the relative address becomes (9 (address) - 3 (address) = +6), and can not be represented with three bits, so that [27] is designated as "High". For D14 and after, a relative address is registered to [26:24], and a fact is registered in [27] whether or not a relative address can be registered.

[0093]

In case of the vertical two pixels adding method of Figure 5, defect pixels to be detected are D5, D6, D1, D2, and the like, and an address of D5 to be first used of the address/defect pixel position memory 40 is designated as address 4 by the start address memory 50. Thus, a relative address (5 (address) - 4 (address) = +1) of D6 of address 5 to be next used is registered in the upper part [26:24] of address 4. While a relative address of D1 of address 0 to be next used is registered in the upper part [26:24] of address 5, the relative address becomes (0 (address) - 5 (address) = -5), and can not be represented with three bits, so that [27] is designated as "High". For D1 and after, a relative address is registered to [26:24], and a fact is registered in [27] whether or not a relative address can be registered.

[0094]

Figure 16 illustrates the start address memory 50 when an imaging element of the vertical simple thinning method of Figure 4 is used, and Figure 17 illustrates the start address memory 50 when an imaging element of the vertical two pixel adding method of Figure 5 is used. When an address error signal is outputted from the address converting unit 60, the start address memory 50 transfers an absolute address to the address converting unit 60 and the address/defect pixel position memory 40.

[0095]

Next, while a detailed configuration and a detailed operation will be described, for the all pixel reading mode,

the configuration and operation are the same as those of the above embodiment 2, the description will be omitted. The detailed configuration and the detailed operation of the high rate reading mode will be described. First, the detailed configuration and the detailed operation of the vertical simple thinning method of Figure 4 will be described. When the high rate reading mode is started by a not-illustrated switch, a not-illustrated shutter, or the like, the timing generator 35 generates a timing clock for driving the imaging element 32.

[0096]

The imaging element 32 outputs an imaging signal depending on the strength of light, and the imaging signal passes through the analog processing unit 33 to be converted to a digital image signal by the A/D converter 34, and is transferred to the defect pixel correcting unit 45. At the same time, when the timing generator 35 generates a pixel clock synchronized to the timing clock, the pixel position measuring unit 36 measures the pixel clock. At this time, in the vertical simple thinning method of Figure 4, by designating eight lines as a unit in a vertical direction, only the second line and the seventh line are read, so that the counter in a vertical direction is measured as indicating absolute positions of one screen as 2, 7, 10, 15, 18, and the like. The measured result is sequentially transferred to the defect pixel detecting unit 43.

[0097]

On the other hand, when the high rate reading mode is started, the address information "address 2" of address 0 of the start address memory 50, i.e., an address of the address/defect pixel position memory 40, at which D3, which is first used in the vertical simple thinning method, is registered, is transferred by the memory controlling circuit 41 to the address/defect pixel position memory 40. The read position information [23:0] of D3 of "address 2" in the address/defect pixel position memory 40 is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42.

[0098]

At the same time, the relative address information ([27] = 0, [26:24] = +1) of "address 2" is transferred to the memory address register 51. Since the 27th bit is "Low", the address converting unit 60 executes an address calculation (2 (address) + 1 = 3 (address)) to be next designated of the address/defect pixel position memory 40 from the address information (address 2) outputted from the start address memory 50. A calculated result "address 3" which becomes an address of D4 is transferred to the memory controlling circuit 41, and it is prepared to read D4 from the address/defect pixel position memory 40. The defect pixel detecting unit 43 compares the defect pixel position register 42 with the measured result which is sequentially transferred from the pixel position measuring unit 36, and when both correspond to each other, outputs the defect pixel detection signal 44. Based on this signal, the defect pixel correcting

unit 45 replaces an image signal of the defect pixel D3 of digital image signals with a value which is linearly interpolated by using an image signal of the two same color factor adjacent pixels in a horizontal direction.

[0099]

At the same time, the defect pixel detection signal 44 outputted from the defect pixel detecting unit 43 is transferred to the memory controlling circuit 41, and the address information "address 3" which is the calculated result by the address converting unit 60 is transferred to an address input of the address/defect pixel position memory 40. Thereby, "address 3" of the address/defect pixel position memory 40, i.e., D4 to be next used in the vertical simple thinning method is read. The read position information [23:0] of D4 of "address 3" in the address/defect pixel position memory 40 is transferred to the defect pixel detecting unit 43 through the defect pixel position register 42.

[0100]

At the same time, the address information ([27] = 1, [26:24] = don't care) of "address 3" is transferred to the memory address register 51. Since the 27th bit is "High", the address converting unit 60 can not generate an absolute address, and outputs the address error signal 61. When receiving the address error signal 61, the start address memory 50 increments an address by one to transfer the address information "address 9" of address 1 to the memory controlling circuit 41 and the address converting unit 60.

The defect pixel detecting unit 43 compares the defect pixel position register 42 with the measured result sequentially transferred from the pixel position measuring unit 36, and when both correspond to each other, outputs the defect pixel detection signal 44 again.

[0101]

As described above, based on the address information of the start address memory 50, the defect pixel position information which is first necessary, and the relative address information which is next necessary are read from the address/defect pixel position memory 40. At the same time, when an absolute address can be generated, the address converting unit 60 calculates an absolute address at which the defect pixel position information to be next detected is registered based on the address information and the relative address information of the start address memory 50, and when the absolute address can not be generated, outputs the address error signal 61 to the start address memory 50 to read a necessary absolute address.

[0102]

Next, such an operation is repeated that the absolute address information of the address converting unit 60 is transferred to the address/defect pixel position memory 40 every time the defect pixel detection signal 44 is outputted. Thereby, the defect pixel position information and the address information are always updated by the defect pixel detection signal 44, and hereinafter, the defect pixels D10,

D14, and the like, and the defect pixels in the vertical simple thinning method are detected and corrected.

[0103]

A configuration and an operation in the vertical two pixel adding method of Figure 5 are the same as those of the above vertical simple thinning method, so that the description will be omitted.

[0104]

As apparent from the above, according to the embodiment 3, by registering a detecting procedure for detecting a defect pixel in the high rate reading mode as a relative address, a memory capacity for the detecting procedure becomes able to be reduced, and it becomes unnecessary to register position information of a defect pixel for the all pixel reading mode and the high rate reading mode respectively, so that a memory capacity can be reduced.

[0105]

Meanwhile, in the embodiment 3, while it is assumed that the imaging element includes 4096-pixel × 4096-row, the number of pixels may be arbitrary, and the number of bits of the pixel counter may be changed depending on the number of pixels. The number of detected defect pixels to be registered may be also arbitrary, and a memory capacity may be changed.

[0106]

In the embodiment 2, while it is assumed that an area is -4 to +3, in which a relative address to be registered can be designated with four-bit, a bit width of the relative

address may be changed in consideration of an interval of a defect pixel to be detected, and the like.

[0107]

The calculating and processing of the address converting unit 60 in the embodiment 3 can be realized by any one of H/W or a microprocessor. Furthermore, while the embodiment 3 is applied to an inputting device, an imaging element, the present invention may be applied to detect a defect pixel of a displaying device such as a liquid crystal and a plasma display, and the same advantageous effect as that of the embodiment 3 may be obtained.

[0108]

[Embodiment 4]

Figure 18 is a configuration diagram illustrating a defect pixel detecting apparatus according to an embodiment 4 of the present invention, and in Figure 18, the same code as that of Figure 1 indicates the same unit as that of Figure 1 or the corresponding unit to that of Figure 1, so that the description will be omitted. Reference numeral 70 denotes a memory registering position information of a defect pixel of 24-bit in total of vertical and horizontal directions, and five-bit identifying flag information detecting defect pixel position information necessary for each mode, and is a flag/defect pixel position memory (memorizing means) which can register a maximum of 256 pieces of defect pixel position information. Reference numerals 71a, 71b, 71c, and 71d are 24-bit position registers which temporarily memorize the defect pixel position information

read from the flag/defect pixel position memory 70. Reference numerals 72a, 72b, 72c, and 72d are five-bit flag registers which temporarily memorize identifying flag information read from the flag/defect pixel position memory 70. Reference numeral 73 is a memory address updating unit which generates an address updating signal of the flag/defect pixel position memory 70, and the like based on flag information outputted from the flag registers 72a, 72b, 72c, and 72d.

[0109]

Next, an operation will be described. In the above embodiments 1 to 3, while the absolute address information or the relative address information is used as a detecting procedure, identifying information may be used as a detecting procedure, which indicates whether or not the defect pixel position information is the defect pixel position information to be detected.

[0110]

An order for registering the defect pixel position information to the flag/defect pixel position memory 70 will be described. In the above embodiments 1 to 3, the defect pixel position information is registered in a memory in order for reading in the all pixel reading mode, that is, in order of Figure 2 in the progressive scan method, and in order of Figure 3 in the field reading method. However, in the embodiment 4 using the identifying information as a detecting procedure, regardless of methods of the all pixel reading mode, the defect pixel position information is registered

in order of left upper to right down of the imaging element 32, that is, in order of Figure 2 as the above embodiments 1 to 3 in the progressive scan method, and in order of Figure 19 in the field reading method.

[0111]

Figure 20 illustrates the flag/defect pixel position memory 70 when an imaging element of the field reading method for four fields is used in the all pixel reading mode, and an imaging element of the vertical simple thinning method of Figure 4 is used in the high rate reading mode. The flag/defect pixel position memory 70 includes eight-bit address space, and can register a maximum of 256 pieces of defect pixel position information. A data width is designated to be 29-bit, and the defect pixel position information is registered in the lower part [23:0] in order of Figure 19. An identifying flag is registered in the upper part [28:24] for the defect pixel position information which is necessary to be detected depending on the reading methods.

[0112]

"High" is registered in the twenty fourth bit to identify defect pixels included in lines which are effective in the high rate reading mode, i.e., D3, D4, D10, D14, and the like included on lines 2, 7, 10, 15, 18, 23, and the like. "High" is registered in the twenty fifth bit to identify defect pixels included in the first field in the all pixel reading mode, i.e., D1, D2, D8, D12, and the like included on lines 1, 5, 9, 13, 17, and the like. Similarly, "High" is registered in the twenty sixth bit to the twenty eighth bit

respectively to identify defect pixels included in the second field to the fourth field.

[0113]

Next, a detailed configuration and a detailed operation will be described by exemplifying the high rate reading mode by the simple thinning method of Figure 4. Since operations of the lens system 31 to the pixel position measuring unit 36, and the defect pixel detecting unit 43 to the defect pixel correcting unit 45 are the same as operations of the simple thinning method in the above embodiments 1 to 3, the description will be omitted.

[0114]

a defect pixel detecting method which is necessary in the high rate reading mode will be described by using both of Figure 21 illustrating the change of the position registers 71a to 71d and the flag registers 72a to 72d, and Figure 22 illustrating a timing chart of the flag/defect pixel position memory 70 in a horizontal retrace line term (corresponding to (1) of Figure 21) immediately after the high rate reading mode is started.

[0115]

When the high rate reading mode is started, the memory controlling circuit 41 identifies one frame of first horizontal retrace line term from a not-illustrated horizontal/vertical synchronization signal, and reads the defect pixel position information and the identifying flag information from address o of the flag/defect pixel position memory 70 in a burst read mode continuously transferring

addresses as illustrated in Figure 22. Next, the memory address updating unit 73 monitors the flag register 72a, and when the twenty fourth bit of the flag/defect pixel position memory 70 is "High", that is, when the defect pixel position information D3 which is necessary in the high rate reading mode is read, activates a burst read mode stop signal to the memory controlling circuit 41, and the reading is stopped. At this time, the defect pixel position information and the identifying flag information of D6 to D3, which are outputted until the reading is actually stopped after the stop signal is activated, are held in the position registers 71a to 71d and the flag registers 72a to 72d as illustrate in (1) of Figure 21.

[0116]

Next, in the high rate reading mode, when a horizontal effective term of the first line, i.e., the second line is started, the defect pixel detecting unit 43 starts comparing the pixel position measuring unit 36 with the position register 71d. When both correspond to each other, that is, the measured result of D3 is outputted from the pixel position measuring unit 36, the defect pixel detection signal 44 is outputted to the memory address updating unit 73. When receiving the defect pixel detection signal 44, the memory address updating unit 73 activates the address updating signal to the memory controlling circuit 41. The memory controlling circuit 41 receives the address updating signal, and reads content of the flag/defect pixel position memory 70 in a single read mode which increments an address by one

to once stops a reading operation. At this time, next defect pixel position information D4 becomes to be held in the position register 71d, and similarly, a defect pixel is detected and the address is updated, and the status becomes (2) of Figure 21.

[0117]

When next horizontal retrace line term, i.e., a horizontal retrace line term of the seventh line is started, the memory address updating unit 73 monitors the status of the flag registers 72a to 72d. In this case, since any one of the flag registers 72a to 72d is "Low", the defect pixel position information and the identifying flag information of the flag/defect pixel position memory 70 are read in the burst read mode as described above, and the status becomes (3) of Figure 21.

[0118]

The pixel position measuring unit 36 executes the measuring for the seventh line and the tenth line, a defect pixel of D10 is detected in the horizontal effective term of the fifteenth line, and the status becomes (4) of Figure 21. When the horizontal retrace line term of the eighteenth line is started in this status, the memory address updating unit 73 again monitors the status of the flag registers 72a to 72d. In this case, since the flag register 72a is "High", and D14 to be next detected is held in the position register 71a, the memory address updating unit 73 provides the memory controlling circuit 41 with an instruction for incrementing

an address by three, and the status becomes (5) of Figure 21.

[0119]

The pixel position measuring unit 36 executes the measuring for the eighteenth line and the twenty third line, a defect pixel of D14 is detected in the horizontal effective term of the twenty sixth line, and the status becomes (6) of Figure 21. As described above, since the memory address updating unit 73 monitors the status of the flag registers 72a to 72d in the horizontal retrace line term, and repeats to control a reading method of the flag/defect pixel position memory 70, a defect pixel becomes able to be detected and corrected in the high rate reading mode.

[0120]

Figure 23 illustrates a controlling flowchart of the above memory address updating unit 73. Here, while the high rate reading mode is designated as a specific example, a defect pixel becomes able to be detected and corrected without depending on the reading mode by controlling to monitor the identifying flag information as described above.

[0121]

As apparent from the above, according to the embodiment 4, by designating a detecting procedure for detecting a defect pixel as the identifying flag information, and controlling a method for reading the flag/defect pixel position memory 70 in the memory address updating unit 73, it becomes unnecessary to register position information of a defect pixel for the all pixel reading mode and the high

rate reading mode respectively, and it becomes possible to control without depending on the reading mode, so that a memory capacity and the size of circuit can be reduced.

[0122]

Meanwhile, in the embodiment 4, while it is assumed that the imaging element includes 4096-pixel × 4096-row, the number of pixels may be arbitrary, and the number of bits of the pixel counter may be changed depending on the number of pixels. The number of detected defect pixels to be registered may be also arbitrary, and a memory capacity may be changed.

[0123]

In the embodiment 4, while the identifying flag information to be registered is designated as five-bit, when the imaging element 32 of the field reading method for two fields is used, the identifying flag information can be realized with three-bit, and when the imaging element 32 of the progressive scan method is used, can be realized with two-bit.

[0124]

The memory address updating unit 73 in the embodiment 4 can be realized by any one of H/W or a microprocessor. Furthermore, while the embodiment 4 is applied to an inputting device, an imaging element, the present invention may be applied to detect a defect pixel of a displaying device such as a liquid crystal and a plasma display, and the same advantageous effect as that of the embodiment 4 may be obtained.

[0125]

[Advantages of the Invention]

As described above, according to the present invention, advantageous effect of the present invention is to obtain an high general-purpose defect pixel detecting apparatus which, can obtain a pixel position of a defect pixel depending on a referring step corresponding to a reading mode adopted by image reading means without sequentially detecting a position of a defect pixel, and can detect a defect pixel by comparing a pixel position of the defect pixel with a read pixel position measured by a measuring means, since a memorizing means which memorizes the pixel position of the defect pixel is caused to memorize a referring step of the pixel position for each reading mode, and can reduce a memory capacity, since it is not necessary to register position information of the defect pixel for each reading mode, and can deal with an imaging element of a variety of reading methods such as the all pixel reading method and the high rate reading method.

[0126]

According to the present invention, advantageous effect of the present invention is that a white dead area and a black dead area can be apparently eliminated since it is configured so that correcting means is provided which corrects an image signal of a defect pixel detected by defect pixel detecting means.

[0127]

According to the present invention, another advantageous effect of the present invention is that a memory capacity can be reduced since it is configured so that a pair of a pixel position and a referring step of defect pixel is memorized.

[0128]

According to the present invention, another advantageous effect of the present invention is that the pixel position of a defect pixel can be quickly identified since it is configured so that the referring step of a pixel position memorized in memorizing means is coordinate information indicating an absolute address at which a pixel position of a defect pixel is memorized.

[0129]

According to the present invention, another advantageous effect of the present invention is that a memory capacity can be reduced since it is configured so that the referring step of a pixel position memorized in the memorizing means is coordinate information indicating a relative address at which a pixel position of a defect pixel is memorized.

[0130]

According to the present invention, another advantageous effect of the present invention is that a memory capacity and the size of circuit can be reduced since it is configured so that the referring step of a pixel position memorized in the memorizing means is identifying information

indicating whether or not the pixel position is a pixel position of a desired defect pixel.

[0131]

According to the present invention, another advantageous effect of the present invention is that a pixel position and the referring step of a defect pixel can be quickly outputted to defect pixel detecting means even when the reading rate from the memorizing means is slow, since it is configured so that temporary storing means is provided which previously reads and temporarily stores the pixel position and the referring step of the defect pixel memorized in the memorizing means, and when the read pixel position is outputted from measuring means, outputs the pixel position and the referring step of the defect pixel to defect pixel detecting means.

[0132]

According to the present invention, another advantageous effect of the present invention is that a pixel position and the referring step of a defect pixel can be quickly outputted to the defect pixel detecting means even when the reading rate from the memorizing means is slow, since it is configured so that the temporary storing means temporarily stores pixel positions and the referring steps of a plurality of defect pixels.

[0133]

According to the present invention, another advantageous effect of the present invention is that a high general-purpose defect pixel detecting apparatus can be

obtained which can deal with imaging elements of a variety of reading methods since it is configured so that a pixel position of a defect pixel is obtained depending on the referring step corresponding to a reading mode adopted by an image reading procedure, and a defect pixel is detected by comparing the pixel position of a defect pixel with a read pixel position measured by a measuring procedure.

[0134]

According to the present invention, advantageous effect of the present invention is that a white dead area and a black dead area can be apparently eliminated since it is configured so that a correcting procedure is provided which corrects an image signal of a defect pixel detected by a defect pixel detecting procedure.

[0135]

According to the present invention, another advantageous effect of the present invention is that a memory capacity can be reduced since it is configured so that a pair of a pixel position and a referring step of a defect pixel is memorized.

[0136]

According to the present invention, another advantageous effect of the present invention is that the pixel position of a defect pixel can be quickly identified since it is configured so that the referring step of a pixel position memorized in a memorizing procedure is coordinate information indicating an absolute address at which a pixel position of a defect pixel is memorized.

[0137]

According to the present invention, another advantageous effect of the present invention is that a memory capacity can be reduced since it is configured so that the referring step of a pixel position memorized in the memorizing procedure is coordinate information indicating a relative address at which a pixel position of a defect pixel is memorized.

[0138]

According to the present invention, another advantageous effect of the present invention is that a memory capacity and the size of circuit can be reduced since it is configured so that the referring step of a pixel position memorized in the memorizing procedure is identifying information indicating whether or not the pixel position is a pixel position of a desired defect pixel.

[0139]

According to the present invention, another advantageous effect of the present invention is that a pixel position of a defect pixel and the referring step can be quickly outputted to defect pixel detecting procedure even when the reading rate from the memorizing procedure is slow, since it is configured so that temporary storing procedure is provided which previously reads and temporarily stores a pixel position and the referring step of a defect pixel memorized in the memorizing procedure, and when the read pixel position is outputted from a measuring procedure,

outputs the pixel position and the referring step of the defect pixel to a defect pixel detecting procedure.

[0140]

According to the present invention, another advantageous effect of the present invention is that a pixel position and the referring step of a defect pixel can be quickly outputted to the defect pixel detecting procedure even when the reading rate from the storing procedure is slow, since it is configured so that the temporary storing procedure temporarily stores pixel positions and the referring steps of a plurality of defect pixels.

[Brief Description of the drawings]

[Figure 1]

Figure 1 is a configuration diagram illustrating a defect pixel detecting apparatus according to an embodiment 1 of the present invention.

[Figure 2]

Figure 2 is an explanatory diagram illustrating a part of an imaging element surface of a progressive scan method in an all pixel reading mode.

[Figure 3]

Figure 3 is an explanatory diagram illustrating a part of an imaging element surface of a field reading method in an all pixel reading mode.

[Figure 4]

Figure 4 is an explanatory diagram illustrating a part of an imaging element surface of a vertical simple thinning method in a high rate reading mode.

[Figure 5]

Figure 5 is an explanatory diagram illustrating a part of an imaging element surface of a vertical two pixel adding method in a high rate reading mode.

[Figure 6]

Figure 6 is an explanatory diagram illustrating a defect pixel position memory.

[Figure 7]

Figure 7 is an explanatory diagram illustrating an address memory in the vertical simple thinning method.

[Figure 8]

Figure 8 is an explanatory diagram illustrating an address memory in the vertical two pixel adding method.

[Figure 9]

Figure 1 is a configuration diagram illustrating a defect pixel detecting apparatus according to an embodiment 2 of the present invention.

[Figure 10]

Figure 10 is an explanatory diagram illustrating an address/defect pixel position memory when an imaging element of the vertical simple thinning method is used.

[Figure 11]

Figure 11 is an explanatory diagram illustrating the address/defect pixel position memory when an imaging element of the vertical two pixel adding method is used.

[Figure 12]

Figure 12 is a timing chart in the vertical two pixel adding method.

[Figure 13]

Figure 13 is a configuration diagram illustrating a defect pixel detecting apparatus according to an embodiment 3 of the present invention.

[Figure 14]

Figure 14 is an explanatory diagram illustrating the address/defect pixel position memory when an imaging element of the vertical simple thinning method is used.

[Figure 15]

Figure 15 is an explanatory diagram illustrating the address/defect pixel position memory when an imaging element of the vertical two pixel adding method is used.

[Figure 16]

Figure 16 is an explanatory diagram illustrating a start address memory when an imaging element of the vertical simple thinning method is used.

[Figure 17]

Figure 17 is an explanatory diagram illustrating the start address memory when an imaging element of the vertical two pixel adding method is used.

[Figure 18]

Figure 18 is a configuration diagram illustrating a defect pixel detecting apparatus according to an embodiment 4 of the present invention.

[Figure 19]

Figure 19 is an explanatory diagram illustrating a registering order of defect pixel position information.

[Figure 20]

Figure 20 is an explanatory diagram illustrating a flag/defect pixel position memory when a field reading method for four fields is used in the all pixel reading mode, and an imaging element of the vertical simple thinning method is used in the high rate reading mode.

[Figure 21]

Figure 21 is an explanatory diagram illustrating the change of a position register and a flag register.

[Figure 22]

Figure 22 is an explanatory diagram illustrating a timing chart of the flag/defect pixel position memory in a horizontal retrace line term immediately after the high rate reading mode is started.

[Figure 23]

Figure 23 is a controlling flowchart of a memory address updating unit.

[Figure 24]

Figure 24 is a configuration diagram illustrating a conventional defect pixel detecting apparatus.

[Description of Symbols]

31 lens system

32 imaging element

33 analog processing unit (image reading means)

34 A/D converter (image reading means)

35 timing generator (measuring means)

36 pixel position measuring unit (measuring means)

40 address/defect pixel position memory (memorizing means)

40a defect pixel position memory (memorizing means)

40b address memory (memorizing means)

41 memory controlling circuit (memorizing means)

42 defect pixel position register (temporary storing means)

43 defect pixel detecting unit (defect pixel detecting means)

44 defect pixel detection signal

45 defect pixel correcting unit (correcting means)

50 start address memory

51 memory address register (temporary storing means)

60 address converter

61 address error signal

70 flag/defect pixel position memory (memorizing means)

71a, 71b, 71c, 71d position register

72a, 72b, 72c, 72d flag register

73 memory address updating unit

Figure 1

32 IMAGING ELEMENT

33 ANALOG PROCESSING UNIT

34 A/D CONVERTER

35 TIMING GENERATOR

36 PIXEL POSITION MEASURING UNIT

40a DEFECT PIXEL POSITION MEMORY

40b ADDRESS MEMORY

41 MEMORY CONTROLLING CIRCUIT

42 DEFECT PIXEL POSITION REGISTER

43 DEFECT PIXEL DETECTING UNIT

45 DEFECT PIXEL CORRECTING UNIT

Figure 6

#1 DEFECT PIXEL POSITION INFORMATION

#2 ADDRESS

Figure 7

#1 ADDRESS INFORMATION OF DEFECT PIXEL POSITION MEMORY

#2 ADDRESS

Figure 8

#1 ADDRESS OF DEFECT PIXEL POSITION MEMORY

#2 ADDRESS

Figure 9

32 IMAGING ELEMENT

33 ANALOG PROCESSING UNIT

34 A/D CONVERTER

35 TIMING GENERATOR

36 PIXEL POSITION MEASURING UNIT

40 ADDRESS/DEFECT PIXEL POSITION MEMORY

41 MEMORY CONTROLLING CIRCUIT

42 DEFECT PIXEL POSITION REGISTER

43 DEFECT PIXEL DETECTING UNIT

45 DEFECT PIXEL CORRECTING UNIT

50 START ADDRESS MEMORY

51 MEMORY ADDRESS REGISTER

Figure 10

#1 ADDRESS INFORMATION

#2 DEFECT PIXEL POSITION INFORMATION

#3 ADDRESS

Figure 11

#1 ADDRESS INFORMATION

#2 DEFECT PIXEL POSITION INFORMATION

#3 ADDRESS

Figure 12

#1 CLOCK

#2 HIGH RATE READING MODE START

#3 START ADDRESS MEMORY

#4 MEMORY CS

#5 MEMORY W

#6 MEMORY ADDRESS BUS

#7 MEMORY DATA BUS
(DEFECT PIXEL POSITION INFORMATION)
#8 MEMORY DATA BUS
(ADDRESS INFORMATION)
#9 REGISTER WRITE ENABLE
#10 DEFECT PIXEL POSITION REGISTER
#11 MEMORY ADDRESS REGISTER
#12 DEFECT PIXEL DETECTION SIGNAL
#13 PIXEL POSITION MEASURED RESULT

Figure 13

32 IMAGING ELEMENT
33 ANALOG PROCESSING UNIT
34 A/D CONVERTER
35 TIMING GENERATOR
36 PIXEL POSITION MEASURING UNIT
40 ADDRESS/DEFECT PIXEL POSITION MEMORY
41 MEMORY CONTROLLING CIRCUIT
42 DEFECT PIXEL POSITION REGISTER
43 DEFECT PIXEL DETECTING UNIT
45 DEFECT PIXEL CORRECTING UNIT
50 START ADDRESS MEMORY
51 MEMORY ADDRESS REGISTER
60 ADDRESS CONVERTER

Figure 14

#1 ADDRESS INFORMATION
#2 DEFECT PIXEL POSITION INFORMATION

#3 ADDRESS

Figure 15

#1 ADDRESS INFORMATION

#2 DEFECT PIXEL POSITION INFORMATION

#3 ADDRESS

Figure 16

#1 ADDRESS INFORMATION OF DEFECT PIXEL POSITION MEMORY

#2 ADDRESS

Figure 17

#1 ADDRESS INFORMATION OF DEFECT PIXEL POSITION MEMORY

#2 ADDRESS

Figure 18

32 IMAGING ELEMENT

33 ANALOG PROCESSING UNIT

34 A/D CONVERTER

35 TIMING GENERATOR

36 PIXEL POSITION MEASURING UNIT

41 MEMORY CONTROLLING CIRCUIT

43 DEFECT PIXEL DETECTING UNIT

45 DEFECT PIXEL CORRECTING UNIT

70 FLAG/DEFECT PIXEL POSITION MEMORY

71a POSITION REGISTER

71b POSITION REGISTER

71c POSITION REGISTER

71d POSITION REGISTER

72a FLAG REGISTER

72b FLAG REGISTER

72c FLAG REGISTER

72d FLAG REGISTER

73 MEMORY ADDRESS UPDATING UNIT

Figure 20

#1 IDENTIFYING INFORMATION

#2 DEFECT PIXEL POSITION INFORMATION

#3 ADDRESS

[24] FLAG OF DEFECT PIXEL INCLUDED IN HIGH RATE READING MODE EFFECTIVE LINE

[25] FLAG OF DEFECT PIXEL INCLUDED IN ALL PIXEL READING FIRST FIELD

[26] FLAG OF DEFECT PIXEL INCLUDED IN ALL PIXEL READING SECOND FIELD

[27] FLAG OF DEFECT PIXEL INCLUDED IN ALL PIXEL READING THIRD FIELD

[28] FLAG OF DEFECT PIXEL INCLUDED IN ALL PIXEL READING FOURTH FIELD

Figure 21

#1 HIGH RATE READING MODE START

#2 HORIZONTAL PERIODIC SIGNAL

#3 SECOND LINE EFFECTIVE TERM

#4 SEVENTH LINE EFFECTIVE TERM

#5 TENTH LINE EFFECTIVE TERM

#6 FIFTEENTH LINE EFFECTIVE TERM

#7 EIGHTEENTH LINE EFFECTIVE TERM

#8 TWENTY THIRD LINE EFFECTIVE TERM

#9 TWENTY SIXTH LINE EFFECTIVE TERM

#10 THIRTY FIRST EFFECTIVE TERM

#11 SECOND LINE RETRACE TERM

#12 SEVENTH LINE RETRACE TERM

#13 TENTH LINE RETRACE TERM

#14 FIFTEENTH LINE RETRACE TERM

#15 EIGHTEENTH LINE RETRACE TERM

#16 TWENTY THIRD LINE RETRACE TERM

#17 TWENTY SIXTH LINE RETRACE TERM

#18 THIRTY FIRST RETRACE TERM

#19 POSITION REGISTER 71A

#20 FLAG REGISTER 72A

Figure 22

#1 CLOCK

#2 HIGH RATE READING MODE START

#3 HORIZONTAL SYNCHRONIZATION SIGNAL

#4 MEMORY CS

#5 MEMORY W

#6 MEMORY ADDRESS BUS

#7 MEMORY DATA BUS
(DEFECT PIXEL POSITION INFORMATION)

#8 MEMORY DATA BUS
(IDENTIFYING INFORMATION)

#9 POSITION REGISTER

(DEFECT PIXEL POSITION INFORMATION)

#10 FLAG REGISTER

(IDENTIFYING INFORMATION)

Figure 23

#1 FLAG REGISTER 72d = MEASURED RESULT?

#2 MEMORY SINGLE READ MODE (ADDRESS + 1)

#3 HORIZONTAL RETRACE LINE TERM?

#4 ANY ONE OF FLAG REGISTERS 72A TO 72D IS "HIGH"?

#5 FLAG REGISTERS 72D = 1?

#6 MEMORY SINGLE READ MODE (ADDRESS + 1)

#7 MEMORY BURST READ MODE (ADDRESS + 1)

#8 FLAG REGISTERS 72A = 1?

#9 STOP MEMORY BURST READ MODE

#10 END

Figure 24

1 MICROCOMPUTER

2 BUS INTERFACE CIRCUIT

3 SHIFT REGISTER

4 SHIFT REGISTER

5 SHIFT REGISTER

6 SHIFT REGISTER

7 SHIFT REGISTER

8 SHIFT REGISTER

9 COUNTER

10 TIMING CLOCK GENERATING CIRCUIT

11 IMAGING ELEMENT DRIVER

12 CCD SENSOR

13 SAMPLE HOLD CIRCUIT

14 OUTPUT SIGNAL PROCESSING CIRCUIT

15 COUNTER

16 COUNTER

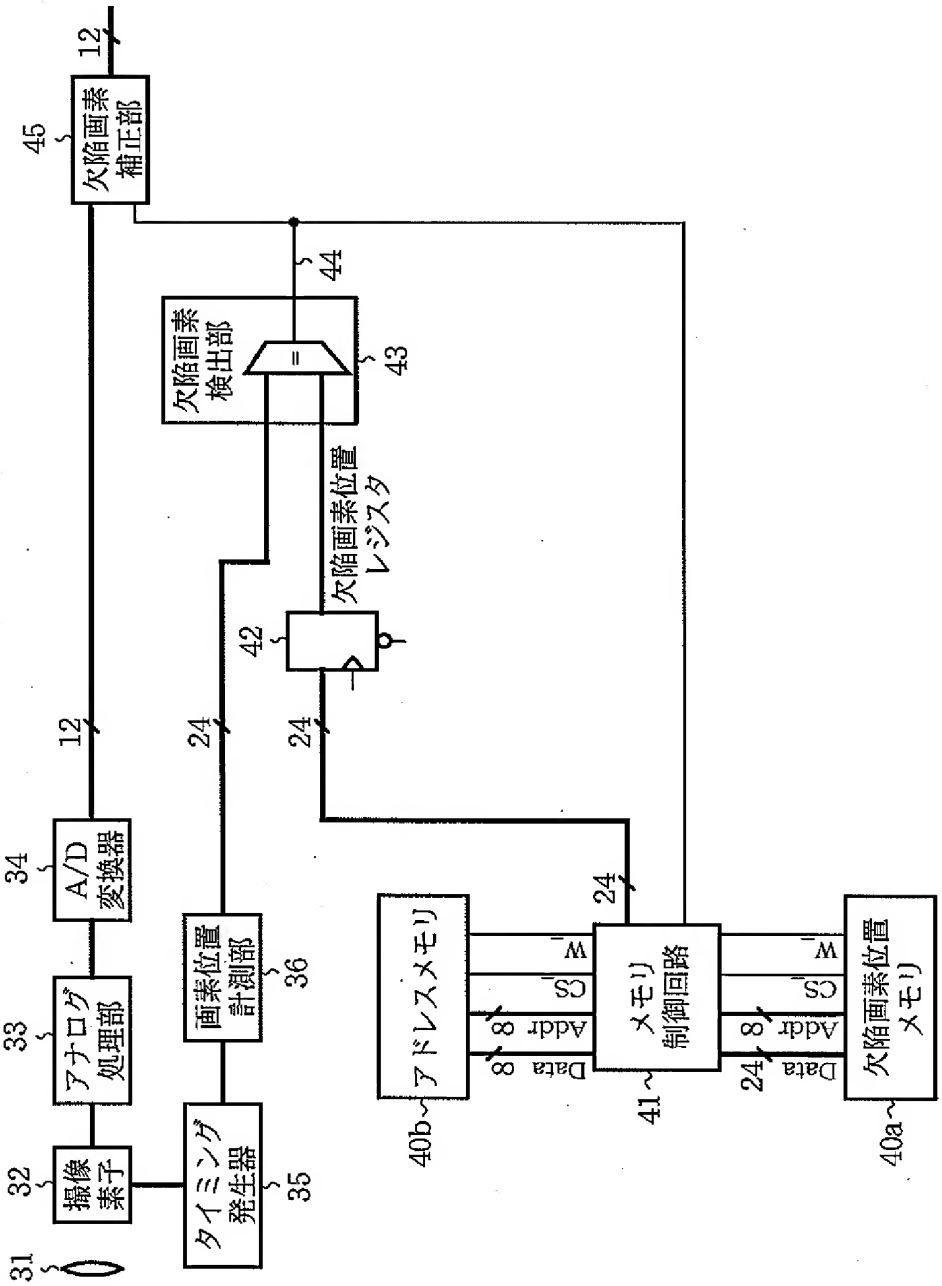
17 COUNTER

18 COMPARATOR

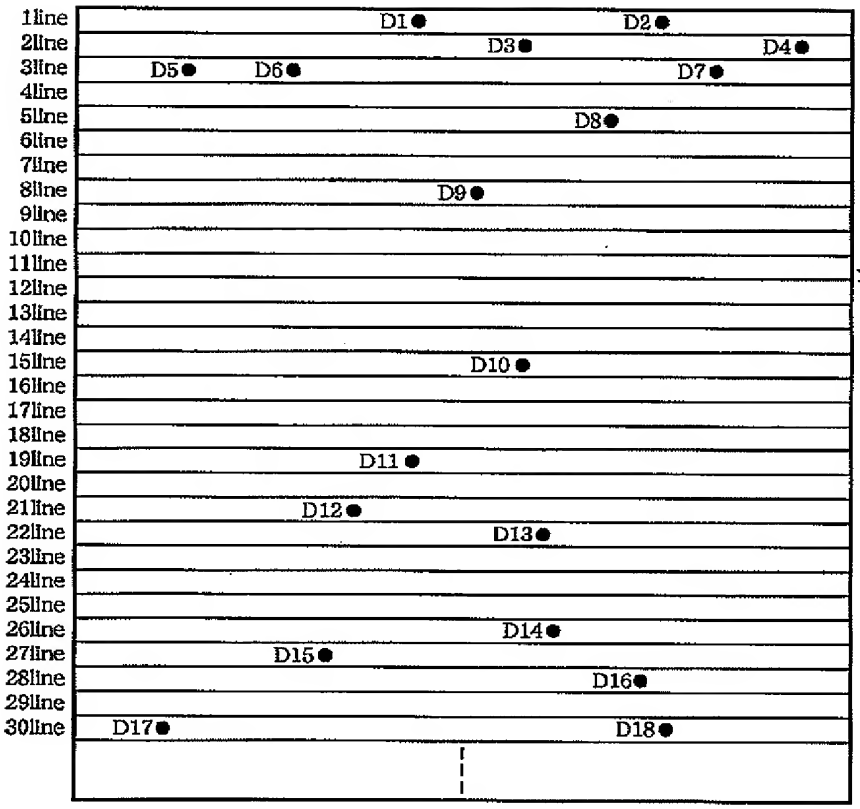
19 COMPARATOR

20 COMPARATOR

【図1】 Fig. 1


31
32
撮像素子
33
アナログ処理部
34
A/D変換器
35
タイミング発生器
36
画素位置計測部
40b
アドレスメモリ
41
メモリ制御回路
40a
欠陥画素位置メモリ
42
43
欠陥画素検出部
44
欠陥画素位置レジスタ
45
欠陥画素補正部
12
24
W
CS
Addr
Data
8

【図２】 Fig. 2



【図６】 Fig. 6

① 欠陥画素位置情報 [23:0]

0	Damage Pixel Adr.D1
1	Damage Pixel Adr.D2
2	Damage Pixel Adr.D3
3	Damage Pixel Adr.D4
4	Damage Pixel Adr.D5
5	Damage Pixel Adr.D6
6	Damage Pixel Adr.D7
7	Damage Pixel Adr.D8
8	Damage Pixel Adr.D9
9	Damage Pixel Adr.D10
10	Damage Pixel Adr.D11
11	Damage Pixel Adr.D12
12	Damage Pixel Adr.D13
13	Damage Pixel Adr.D14
14	Damage Pixel Adr.D15
15	Damage Pixel Adr.D16
16	Damage Pixel Adr.D17
17	Damage Pixel Adr.D18
.	.
.	.

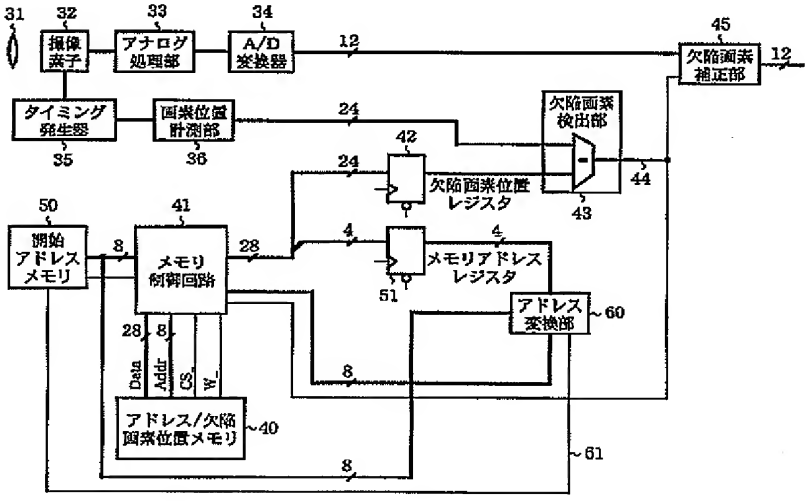
【図７】 Fig. 7

① 欠陥画素位置メモリのアドレス情報[7:0]

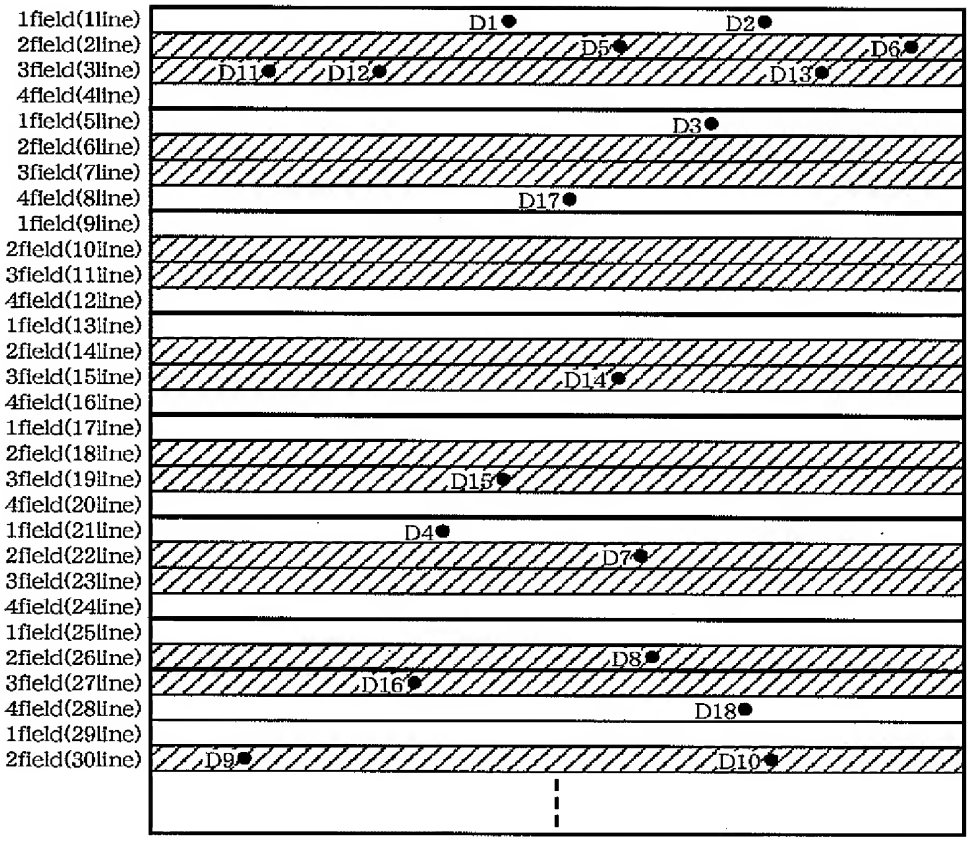
0	Mem.Adr.2
1	Mem.Adr.3
2	Mem.Adr.9
3	Mem.Adr.13
4	.
5	.
6	.
7	.
8	.
9	.
10	.
11	.
12	.
13	.
14	.
15	.
16	.
17	.
.	.
.	.

② アドレス [7:0]

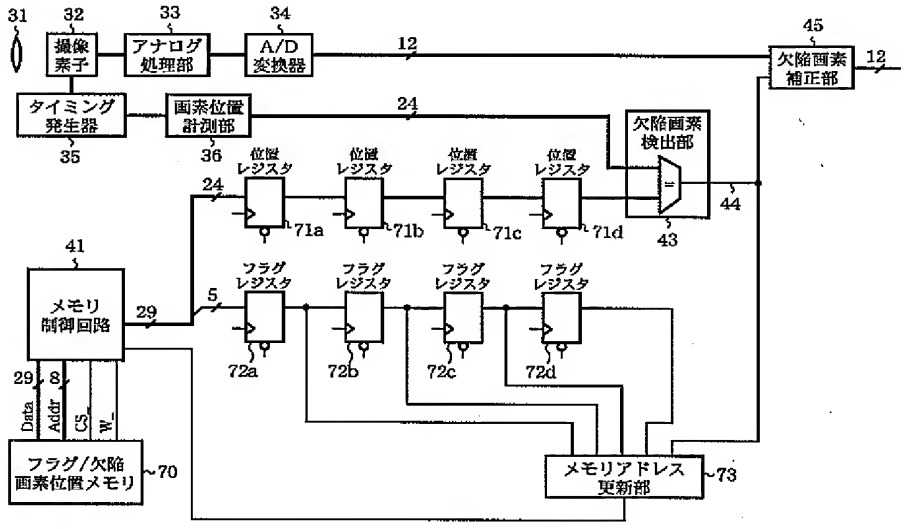
【図１３】 Fig. 13



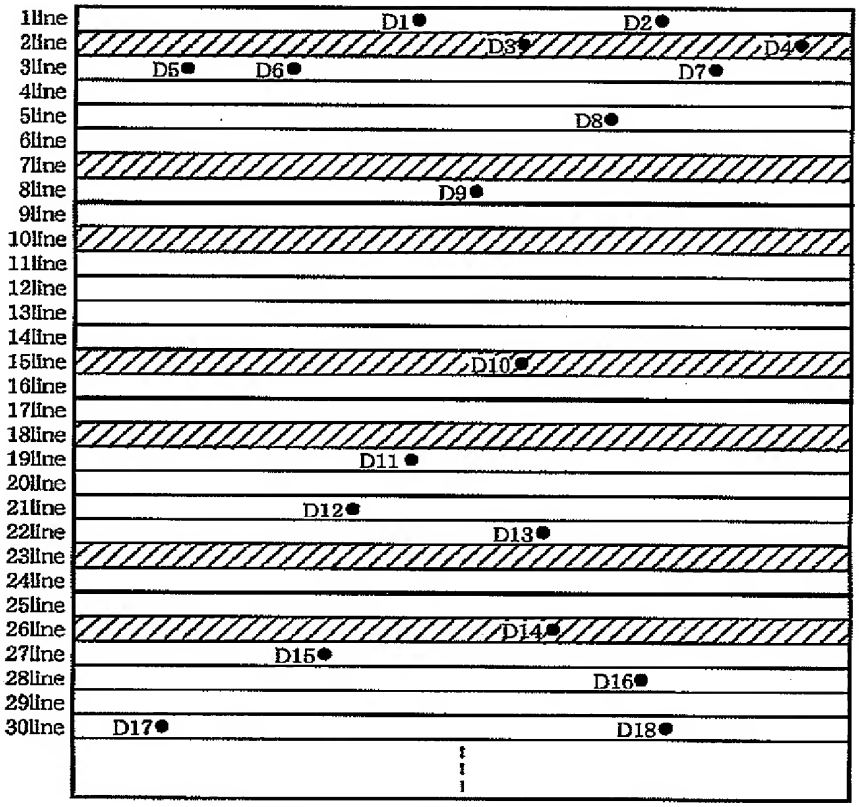
【図３】 Fig. 3



【図１８】 Fig. 18



【図４】 Fig.4



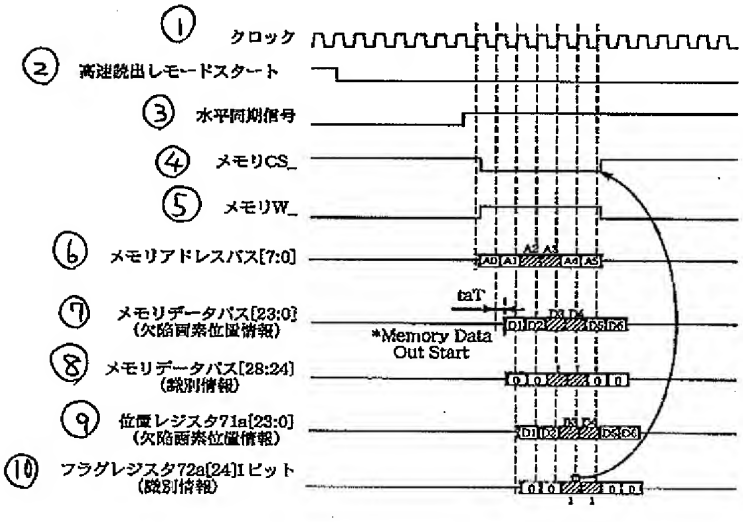
【図８】 Fig.8

	① 欠陥画素位置メモリのアドレス[7:0]
② アドレス[7:0] 0	Mem.Adr.4
1	Mem.Adr.5
2	Mem.Adr.0
3	Mem.Adr.1
4	Mem.Adr.6
5	Mem.Adr.8
6	Mem.Adr.9
7	Mem.Adr.12
8	Mem.Adr.14
9	・
10	・
11	・
12	・
13	・
14	・
15	・
16	・
17	・
・	・
・	・

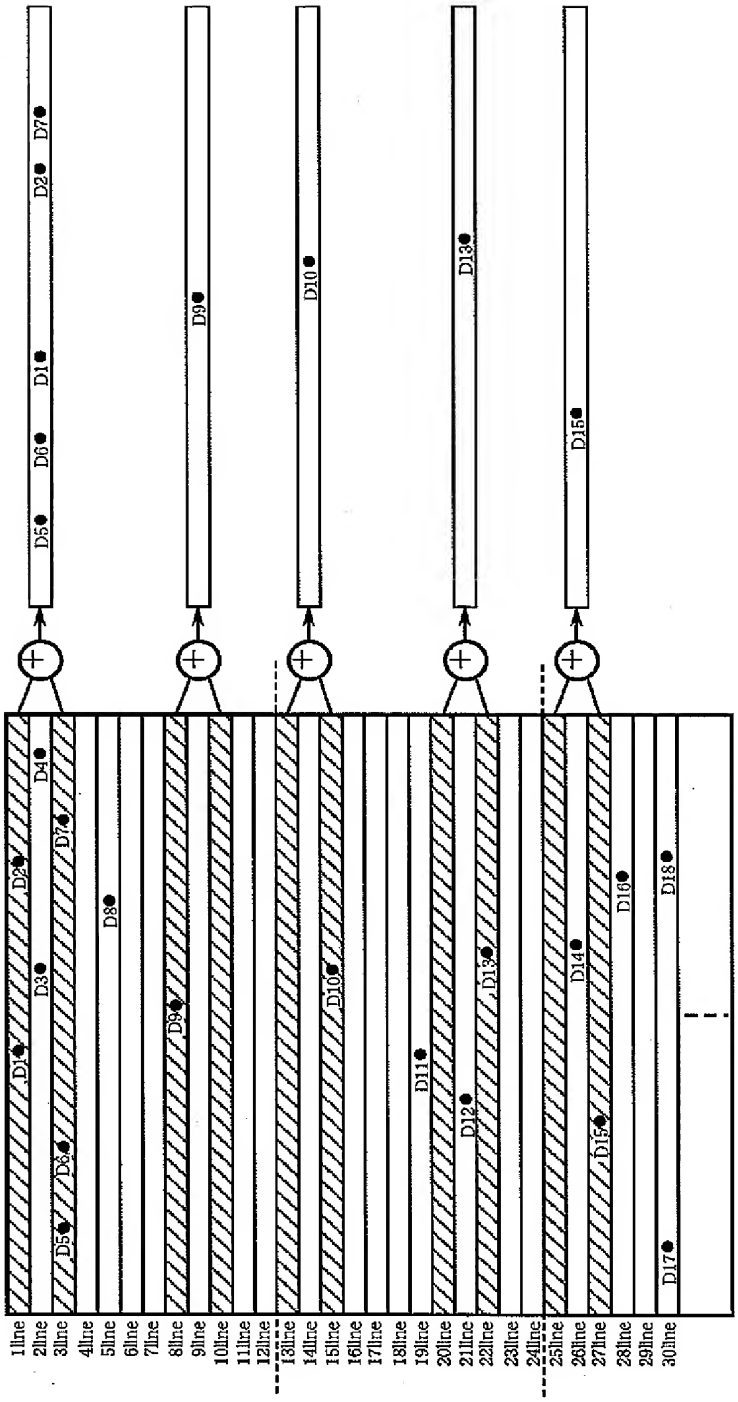
【図１６】 Fig.16

	① 欠陥画素位置メモリのアドレス情報[7:0]
② アドレス[7:0] 0	Mem.Adr.2
1	Mem.Adr.9
2	Mem.Adr.13
3	・
4	・
5	・
6	・
7	・
8	・
9	・
10	・
11	・
12	・
13	・
14	・
15	・
16	・
17	・
・	・
・	・

【図２２】 Fig.22



【図５】 Fig. 5


D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
1line
2line
3line
4line
5line
6line
7line
8line
9line
10line
11line
12line
13line
14line
15line
16line
17line
18line
19line
20line
21line
22line
23line
24line
25line
26line
27line
28line
29line
30line

【図１０】 Fig.10

③アドレス [7:0]	①アドレス情報 [31:24]	②欠陥画素位置情報 [23:0]
0		Damage Pixel Adr.D1
1		Damage Pixel Adr.D2
2	Mem.Adr.3	Damage Pixel Adr.D3
3	Mem.Adr.9	Damage Pixel Adr.D4
4		Damage Pixel Adr.D5
5		Damage Pixel Adr.D6
6		Damage Pixel Adr.D7
7		Damage Pixel Adr.D8
8		Damage Pixel Adr.D9
9	Mem.Adr.13	Damage Pixel Adr.D10
10		Damage Pixel Adr.D11
11		Damage Pixel Adr.D12
12		Damage Pixel Adr.D13
13	Mem.Adr.X	Damage Pixel Adr.D14
14		Damage Pixel Adr.D15
15		Damage Pixel Adr.D16
16		Damage Pixel Adr.D17
17		Damage Pixel Adr.D18
・	・	・
・	・	・

【図１１】 Fig.11

③アドレス [7:0]	①アドレス情報 [31:24]	②欠陥画素位置情報 [23:0]
0	Mem.Adr.1	Damage Pixel Adr.D1
1	Mem.Adr.6	Damage Pixel Adr.D2
2		Damage Pixel Adr.D3
3		Damage Pixel Adr.D4
4	Mem.Adr.5	Damage Pixel Adr.D5
5	Mem.Adr.0	Damage Pixel Adr.D6
6	Mem.Adr.8	Damage Pixel Adr.D7
7		Damage Pixel Adr.D8
8	Mem.Adr.9	Damage Pixel Adr.D9
9	Mem.Adr.12	Damage Pixel Adr.D10
10		Damage Pixel Adr.D11
11		Damage Pixel Adr.D12
12	Mem.Adr.14	Damage Pixel Adr.D13
13		Damage Pixel Adr.D14
14	Mem.Adr.X	Damage Pixel Adr.D15
15		Damage Pixel Adr.D16
16		Damage Pixel Adr.D17
17		Damage Pixel Adr.D18
・	・	・
・	・	・

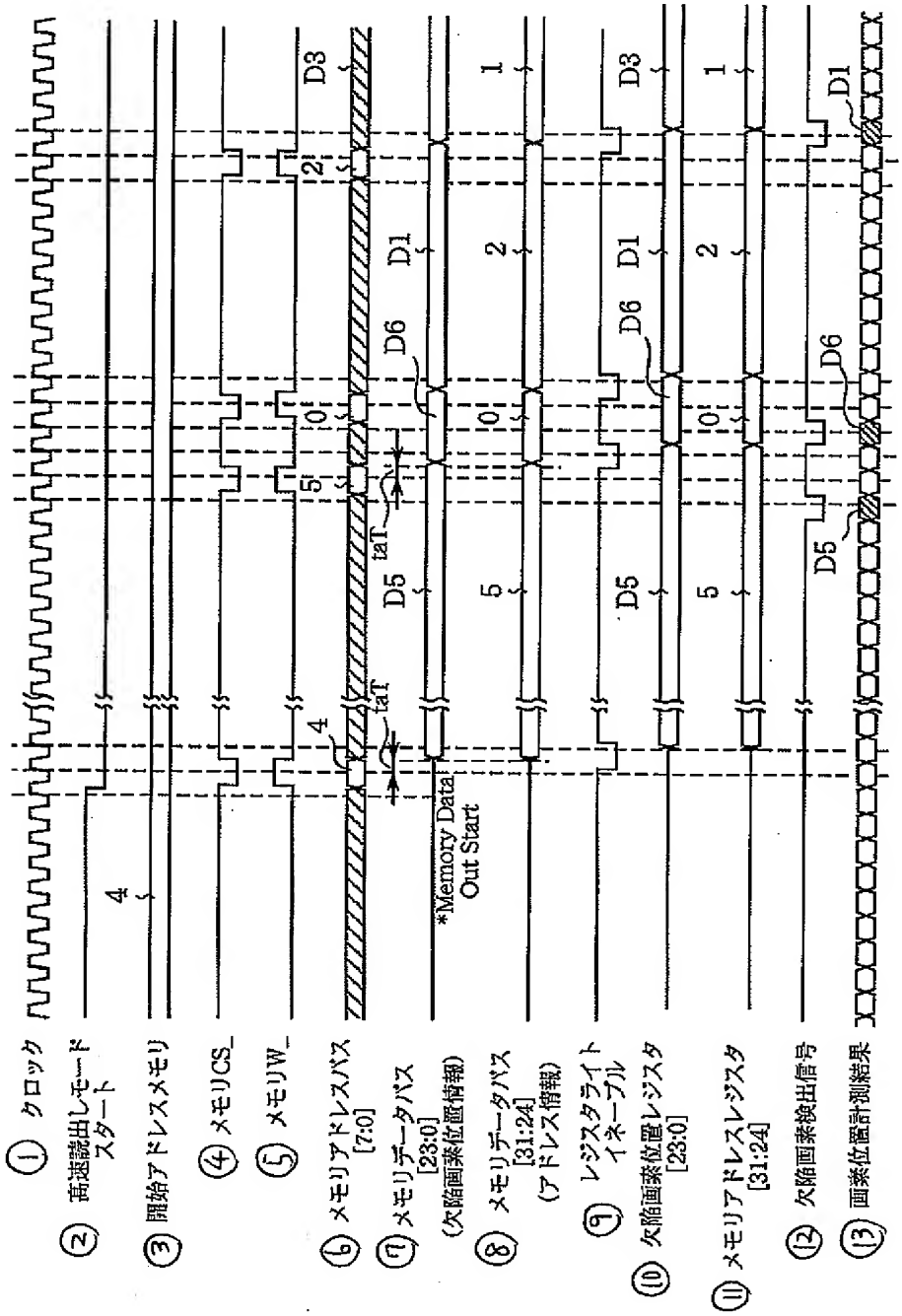
【図１４】 Fig.14

③アドレス [7:0]	①[27]	①アドレス情報 [26:24]	②欠陥画素位置情報 [23:0]
0			Damage Pixel Adr.D1
1			Damage Pixel Adr.D2
2	0	+1	Damage Pixel Adr.D3
3	1	don't care	Damage Pixel Adr.D4
4			Damage Pixel Adr.D5
5			Damage Pixel Adr.D6
6			Damage Pixel Adr.D7
7			Damage Pixel Adr.D8
8			Damage Pixel Adr.D9
9	1	don't care	Damage Pixel Adr.D10
10			Damage Pixel Adr.D11
11			Damage Pixel Adr.D12
12			Damage Pixel Adr.D13
13	1	don't care	Damage Pixel Adr.D14
14			Damage Pixel Adr.D15
15			Damage Pixel Adr.D16
16			Damage Pixel Adr.D17
17			Damage Pixel Adr.D18
・		・	・
・		・	・

【図１５】 Fig.15

③アドレス [7:0]	①[27]	①アドレス情報 [26:24]	②欠陥画素位置情報 [23:0]
0	0	+1	Damage Pixel Adr.D1
1	1	don't care	Damage Pixel Adr.D2
2			Damage Pixel Adr.D3
3			Damage Pixel Adr.D4
4	0	+1	Damage Pixel Adr.D5
5	1	don't care	Damage Pixel Adr.D6
6	0	+2	Damage Pixel Adr.D7
7			Damage Pixel Adr.D8
8	0	+1	Damage Pixel Adr.D9
9	0	+3	Damage Pixel Adr.D10
10			Damage Pixel Adr.D11
11			Damage Pixel Adr.D12
12	0	+2	Damage Pixel Adr.D13
13			Damage Pixel Adr.D14
14	1	don't care	Damage Pixel Adr.D15
15			Damage Pixel Adr.D16
16			Damage Pixel Adr.D17
17			Damage Pixel Adr.D18
・		・	・
・		・	・

【図１２】　Fig.12


① クロック
② 高速読出しモード スタート
③ 開始アドレスメモリ
④ メモリCS_
⑤ メモリW_
⑥ メモリアドレスバス [7:0]
⑦ メモリデータバス [23:0] (欠陥画素位置情報)
⑧ メモリデータバス [31:24] (アドレス情報)
⑨ レジスタライト イネーブル
⑩ 欠陥画素位置レジスタ [23:0]
⑪ メモリアドレスレジスタ [31:24]
⑫ 欠陥画素検出信号
⑬ 画素位置計測結果
*Memory Data Out Start
taT
D1
D3
D5
D6
0
1
2
4
5

【図１７】 Fig.17

② アドレス [7:0]

	① 欠陥画素位置メモリのアドレス情報[7:0]
0	Mem.Adr.4
1	Mem.Adr.0
2	Mem.Adr.6
3	・
4	・
5	・
6	・
7	・
8	・
9	・
10	・
11	・
12	・
13	・
14	・
15	・
16	・
17	・
・	・
・	・

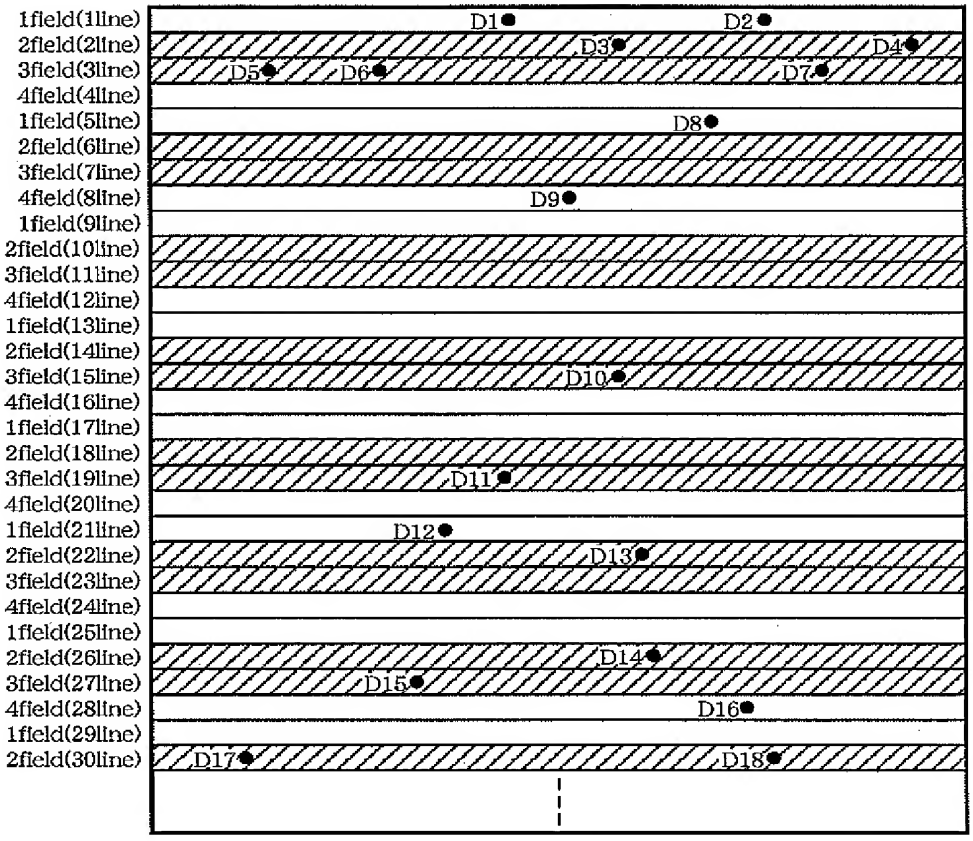
【図２０】 Fig.20

③ アドレス [7:0]

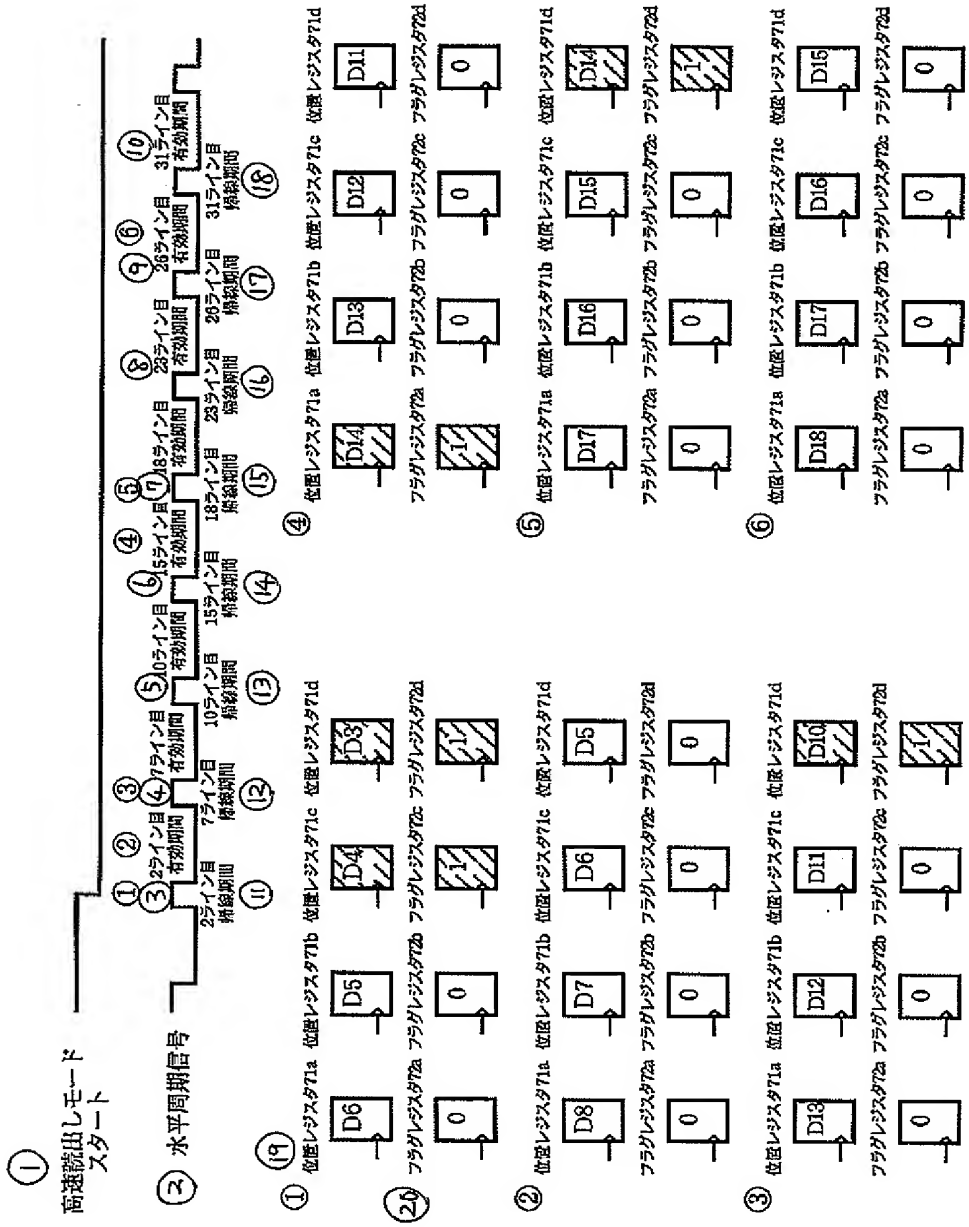
	① 識別情報 [28:24]					② 欠陥画素位置情報 [23:0]
0	0	0	0	1	0	Damage Pixel Adr.D1
1	0	0	0	1	0	Damage Pixel Adr.D2
2	0	0	1	0	1	Damage Pixel Adr.D3
3	0	0	1	0	1	Damage Pixel Adr.D4
4	0	1	0	0	0	Damage Pixel Adr.D5
5	0	1	0	0	0	Damage Pixel Adr.D6
6	0	1	0	0	0	Damage Pixel Adr.D7
7	0	0	0	1	0	Damage Pixel Adr.D8
8	1	0	0	0	0	Damage Pixel Adr.D9
9	0	1	0	0	1	Damage Pixel Adr.D10
10	0	1	0	0	0	Damage Pixel Adr.D11
11	0	0	0	1	0	Damage Pixel Adr.D12
12	0	0	1	0	0	Damage Pixel Adr.D13
13	0	0	1	0	1	Damage Pixel Adr.D14
14	0	1	0	0	0	Damage Pixel Adr.D15
15	1	0	0	0	0	Damage Pixel Adr.D16
16	0	0	1	0	0	Damage Pixel Adr.D17
17	0	0	1	0	0	Damage Pixel Adr.D18
・	・	・	・	・	・	・
・	・	・	・	・	・	・

[24]：高速読出しモード有効ラインに存在する欠陥画素のグラフ
[25]：全画素読出し第一フィールドに存在する欠陥画素のグラフ
[26]：全画素読出し第二フィールドに存在する欠陥画素のグラフ
[27]：全画素読出し第三フィールドに存在する欠陥画素のグラフ
[28]：全画素読出し第四フィールドに存在する欠陥画素のグラフ

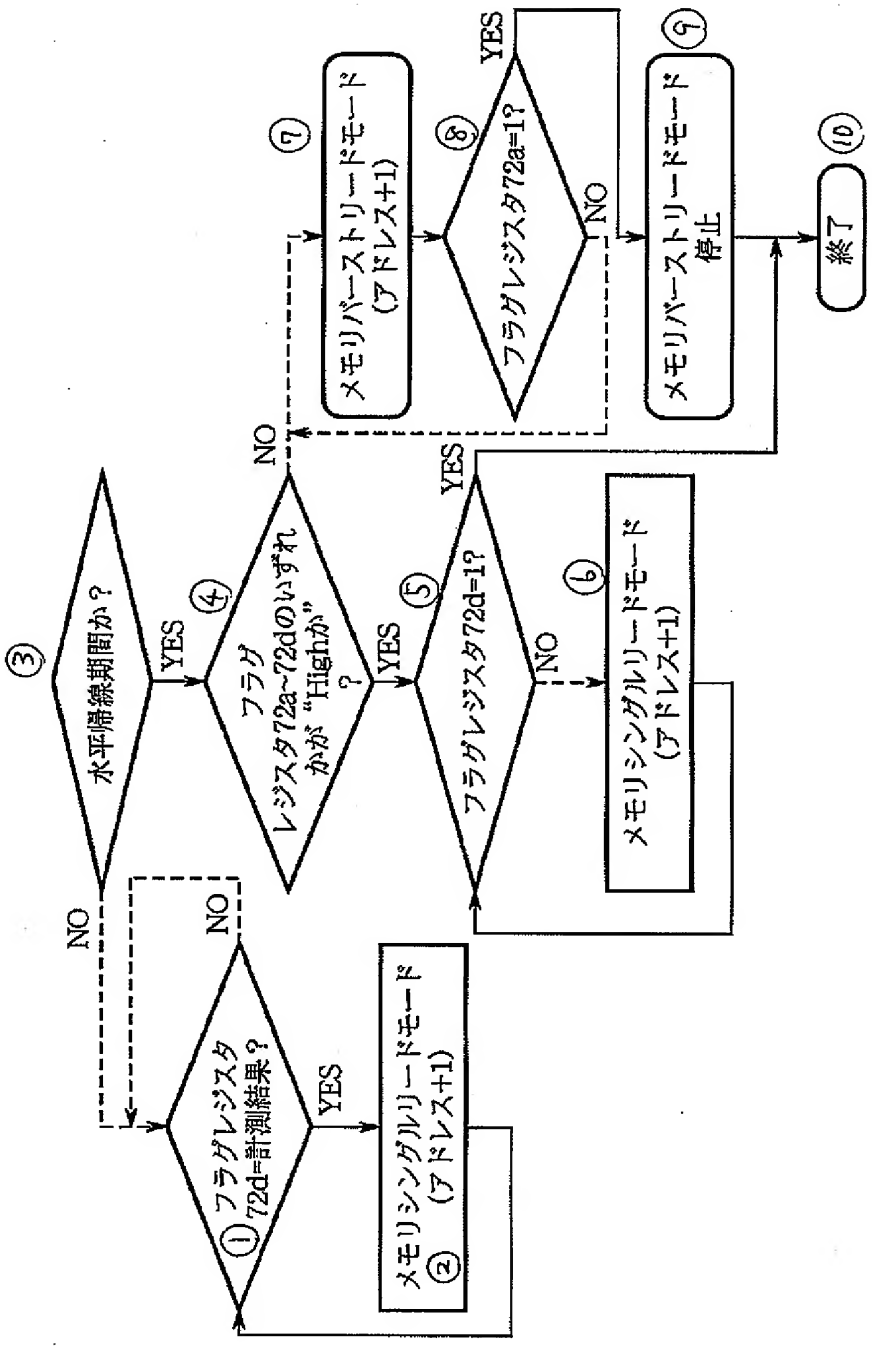
【図１９】 Fig. 19


1field(1line)
2field(2line)
3field(3line)
4field(4line)
1field(5line)
2field(6line)
3field(7line)
4field(8line)
1field(9line)
2field(10line)
3field(11line)
4field(12line)
1field(13line)
2field(14line)
3field(15line)
4field(16line)
1field(17line)
2field(18line)
3field(19line)
4field(20line)
1field(21line)
2field(22line)
3field(23line)
4field(24line)
1field(25line)
2field(26line)
3field(27line)
4field(28line)
1field(29line)
2field(30line)
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18

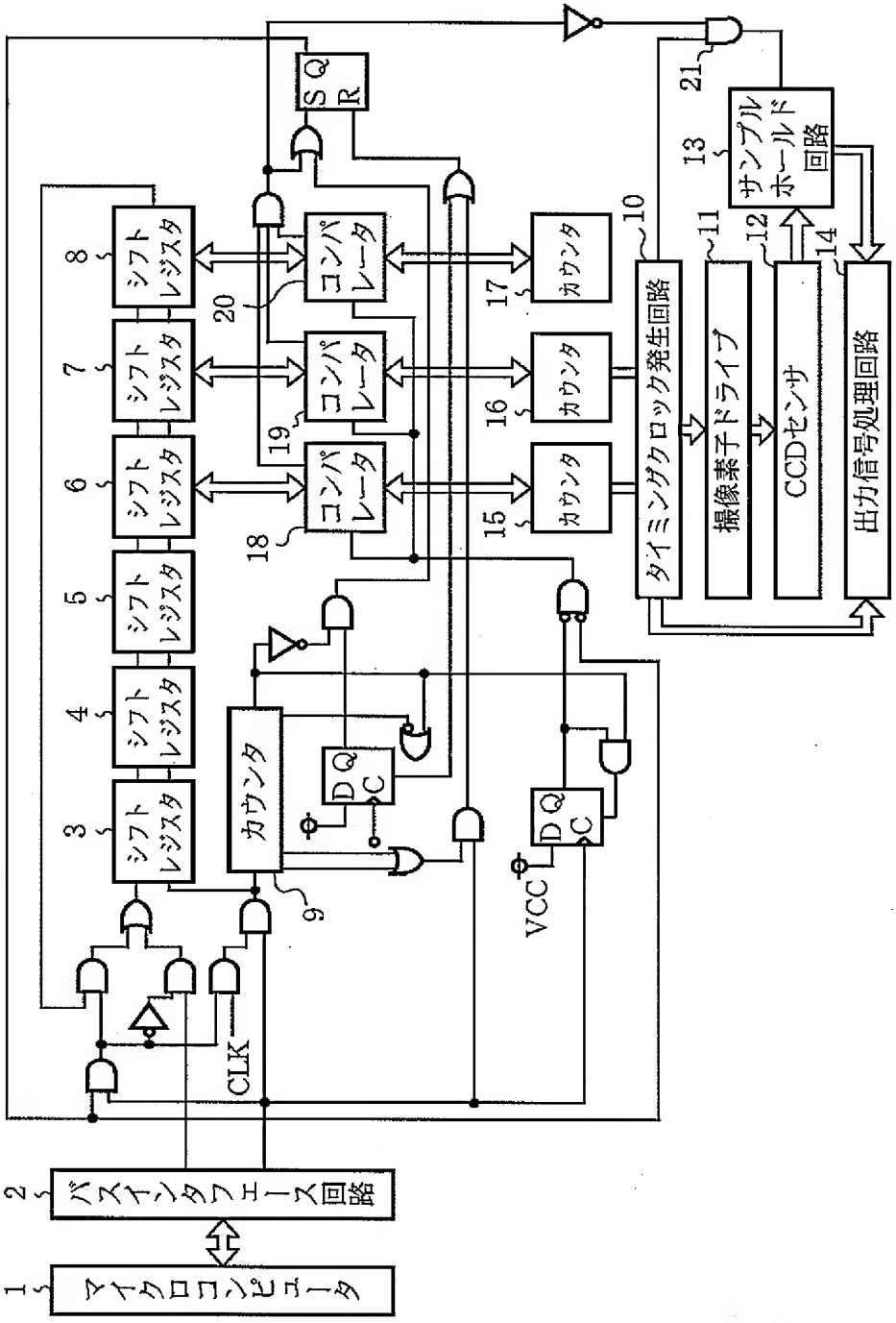
【図21】　Fig. 21


高速読出しモード スタート
水平同期信号
2ライン目 有効期間
2ライン目 休止期間
7ライン目 有効期間
7ライン目 休止期間
10ライン目 有効期間
10ライン目 休止期間
15ライン目 有効期間
15ライン目 休止期間
18ライン目 有効期間
18ライン目 休止期間
23ライン目 有効期間
23ライン目 休止期間
26ライン目 有効期間
26ライン目 休止期間
31ライン目 有効期間
31ライン目 休止期間
位置レジスタ1a
位置レジスタ1b
位置レジスタ1c
位置レジスタ1d
フラグレジスタ2a
フラグレジスタ2b
フラグレジスタ2c
フラグレジスタ2d
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18

【図２３】 Fig. 23


③
水平帰線期間か？
NO
YES
④
フラグ
レジスタ72a~72dのいずれ
かが"High"
か？
NO
YES
⑤
フラグレジスタ72d=1?
NO
YES
⑥
メモリシングルリードモード
(アドレス+1)
⑦
メモリバーストリードモード
(アドレス+1)
⑧
フラグレジスタ72a=1?
NO
YES
⑨
メモリバーストリードモード
停止
⑩
終了
①
フラグレジスタ
72d=計測結果？
NO
YES
②
メモリシングルリードモード
(アドレス+1)

【図２４】 Fig. 24


マイクロコンピュータ
バスインタフェース回路
CLK
シフトレジスタ
コンパレータ
カウンタ
S
Q
R
D
C
VCC
タイミングクロック発生回路
撮像素子ドライブ
CCDセンサ
サンプルホールド回路
出力信号処理回路